
Data volume study

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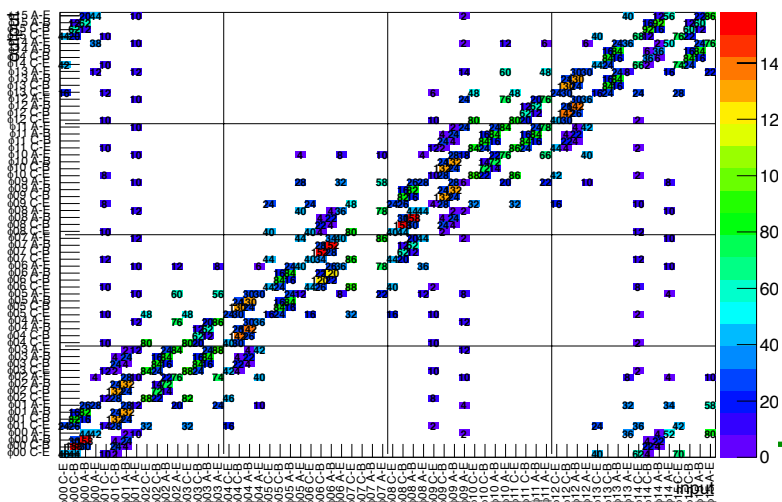
SCT Cabling

ϕ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A Endcap	66	55 60	64 56	48	49	57	61 45	50	65	51 58	52 63	46	59	53 67	47 54	62
A Barrel	2 42	4	6	34 8	10	12 36		14 16	18 44	20	22	38 24	26	40	28	32 30

ϕ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C Endcap	89	72 81	85 73	68	78	84	86 71	79	90	76 83	77 70	88	82	74 80	69 75	87
C Barrel	1 41	3	5	33 7	9	11 35		13 15	17 43	19	21	37 23	25	39	27	31 29

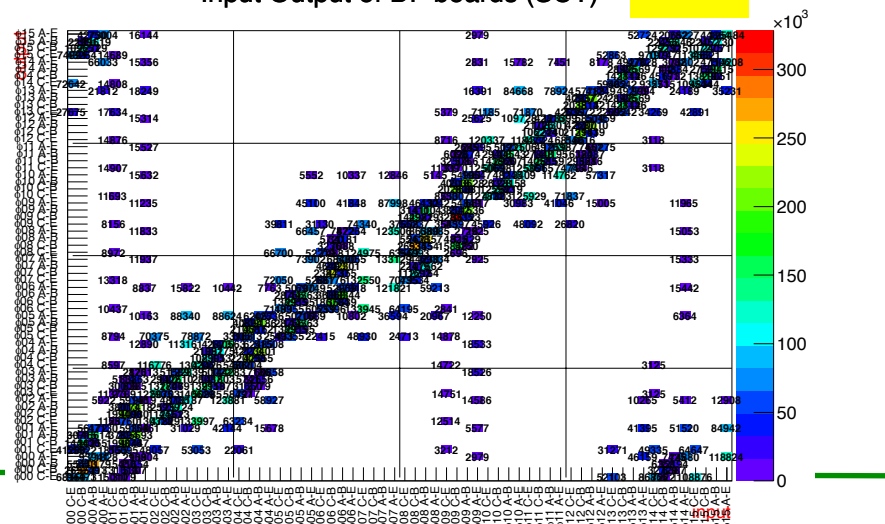
Input Output of DF boards (SCT)

Module



Input Output of DF boards (SCT)

Hit



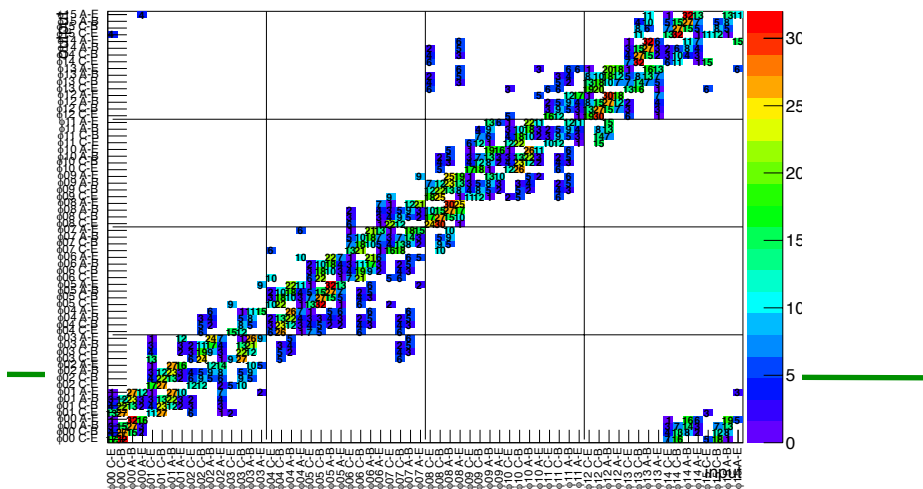
1000Event Integrated @ Pileup7.3

Pixel Cabling

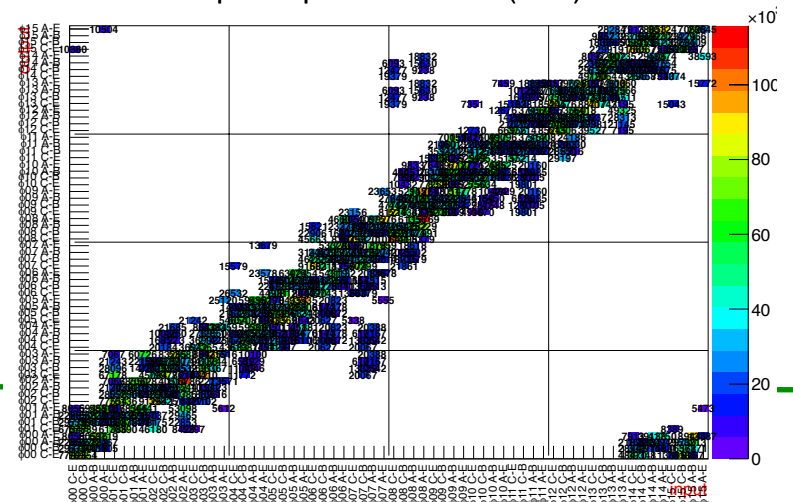
ϕ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A Endcap	60 34	43 35	58 68	56 39	42 19	22 23	54 66 26	27 109 111	52 30	64 2	50 3	6 88	7 10	11 14	48 62	46 18
A Barrel	101 91	117 119	38 93	103 95	105 97	107 99	121 123	71 69	31 86	125 73	90 127	75 77	113 79	129 81	15 131	115 83

ϕ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C Endcap	59 33	44 36	57 67	55 40	41 20	21 24	53 65 25	28 110 112	51 29	63 1	49 4	5 87	8 9	12 13	47 61	45 17
C Barrel	102 92	118 120	37 94	104 96	106 98	108 100	122 124	72 70	32 85	126 74	89 128	76 78	114 80	130 82	16 132	116 84

Input Output of DF boards (Pixel)



Input Output of DF boards (Pixel)



Data volume study

Study how many hits sent from a FPGA to a FPGA with given cabling:

case0: Directly to AUX cards

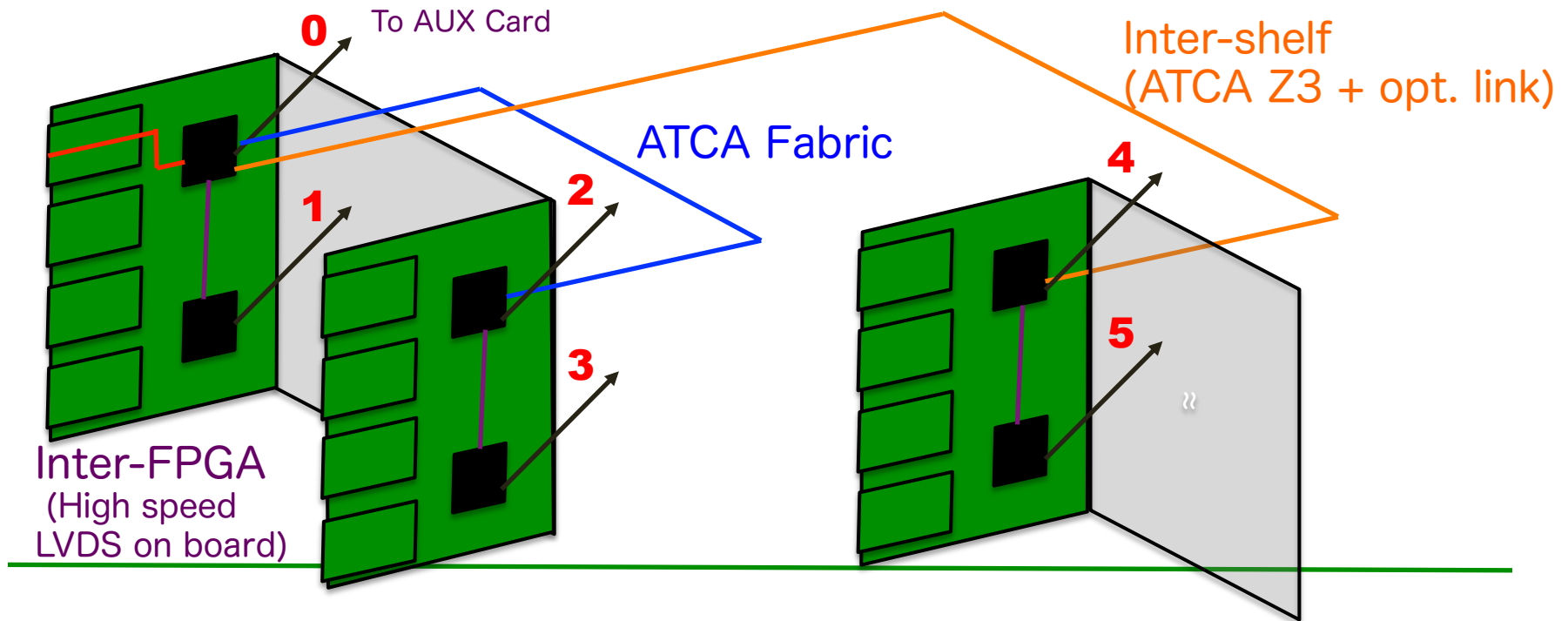
case1: Via Inter-FPGA connection on board

case2: Via ATCA Fabric

case3: Via ATCA Fabric + Inter-FPGA

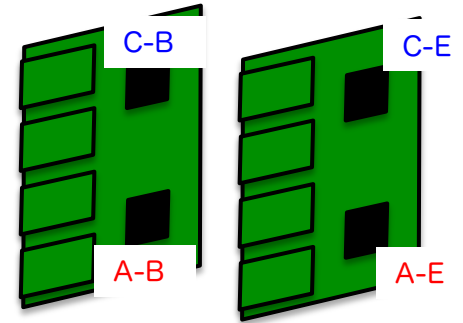
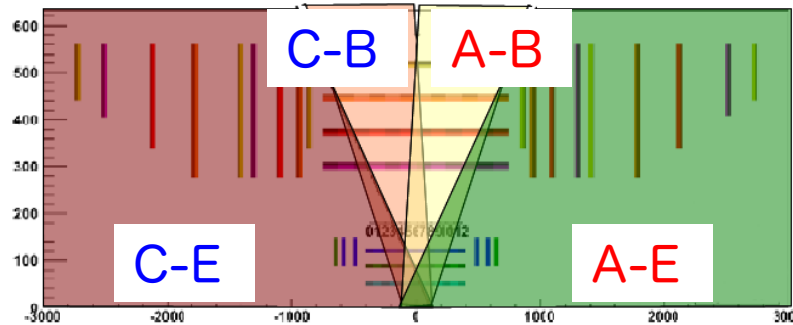
case4: Via Inter-shelf connection (+ with ATCA Fabric)

case5: Via Inter-shelf + Inter-FPGA (+ with ATCA Fabric)

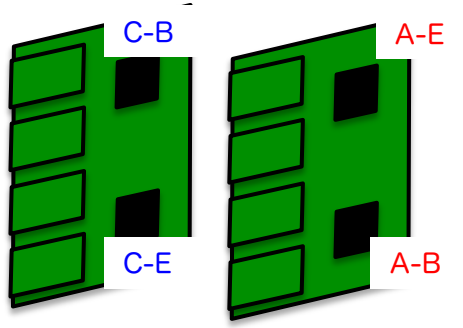
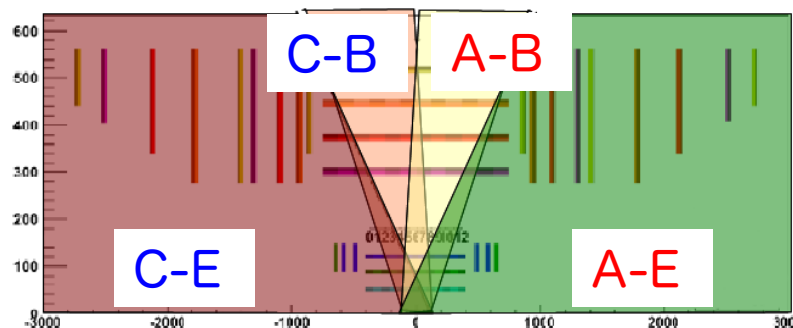


Board alignment plans

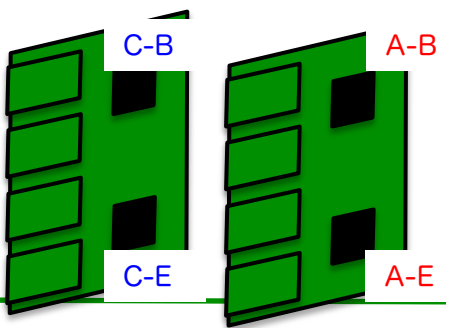
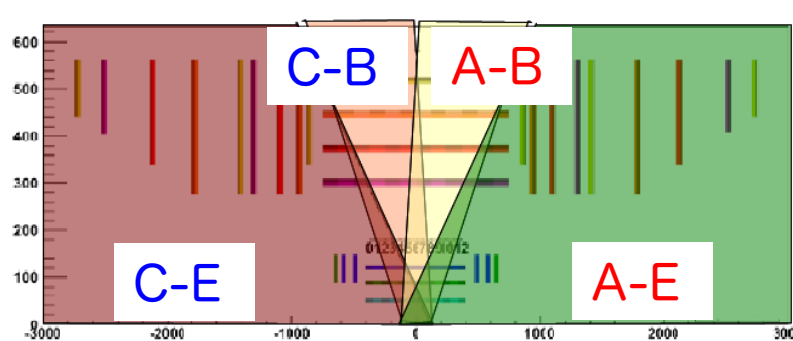
Scenario1



Scenario2



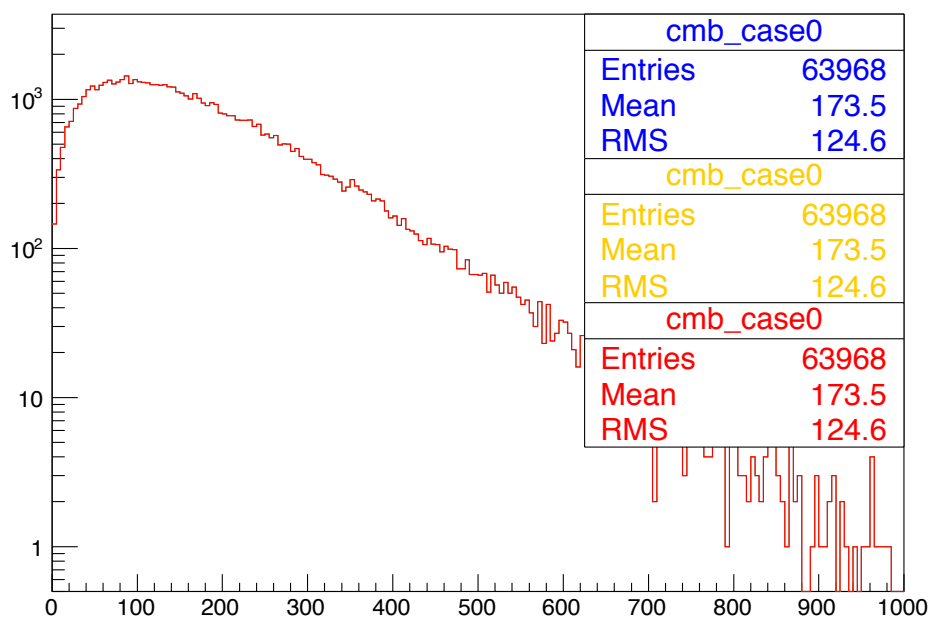
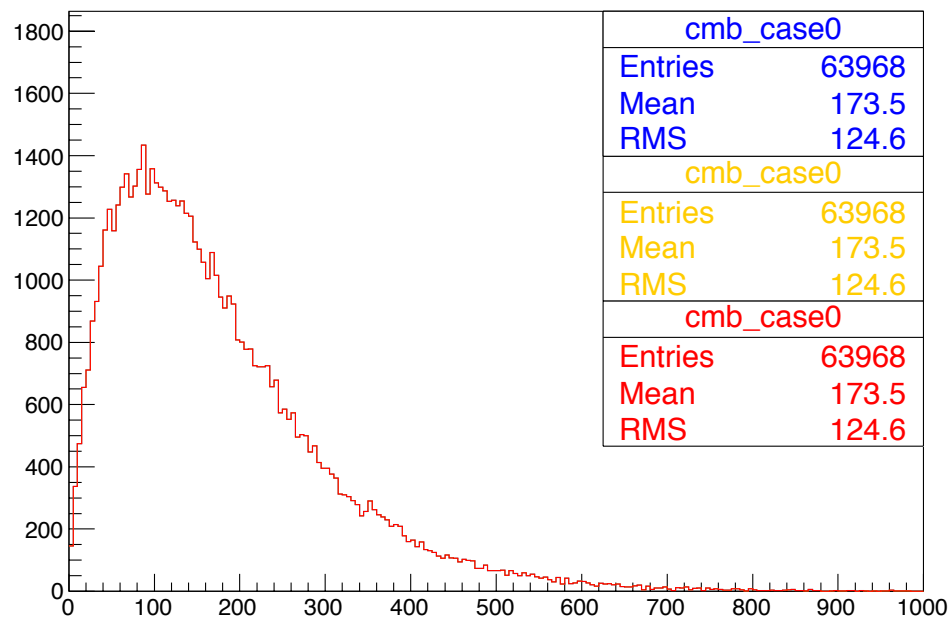
Scenario3



Case0

Directly go to AUX

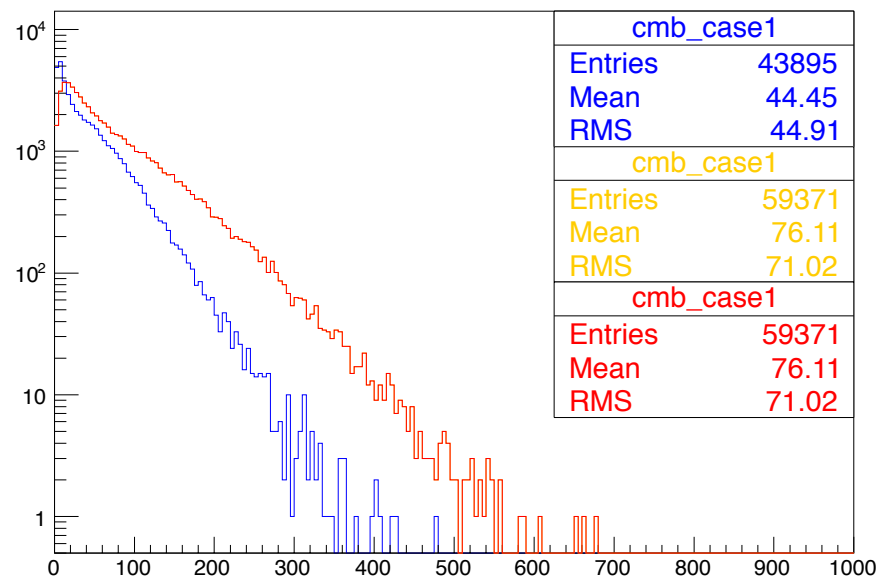
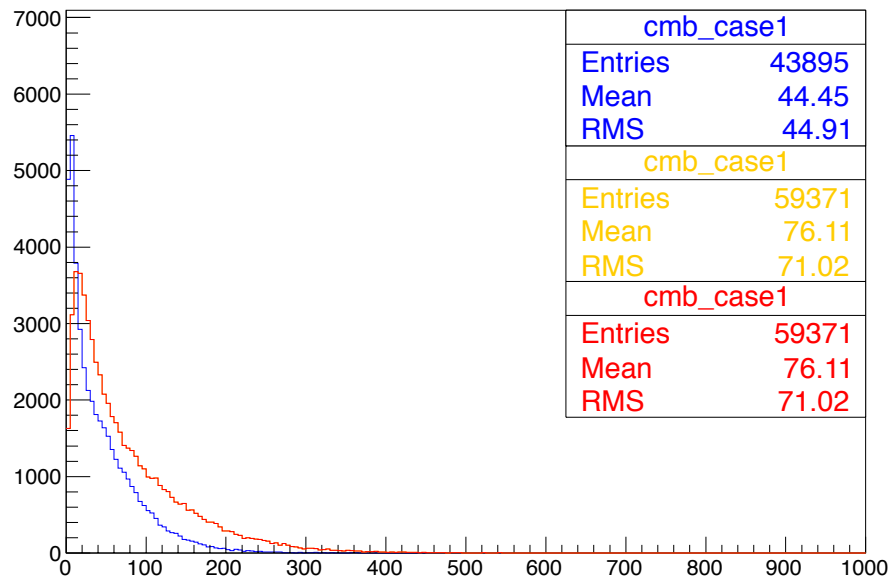
- **Scenario1**: e.g.) C-B $\rightarrow$ C-B, C-E $\rightarrow$ C-E
- **Scenario2**: e.g.) C-B $\rightarrow$ C-B, C-E $\rightarrow$ C-E
- **Scenario3**: e.g.) C-B $\rightarrow$ C-B, C-E $\rightarrow$ C-E



Case1

Inter-FPGA communication

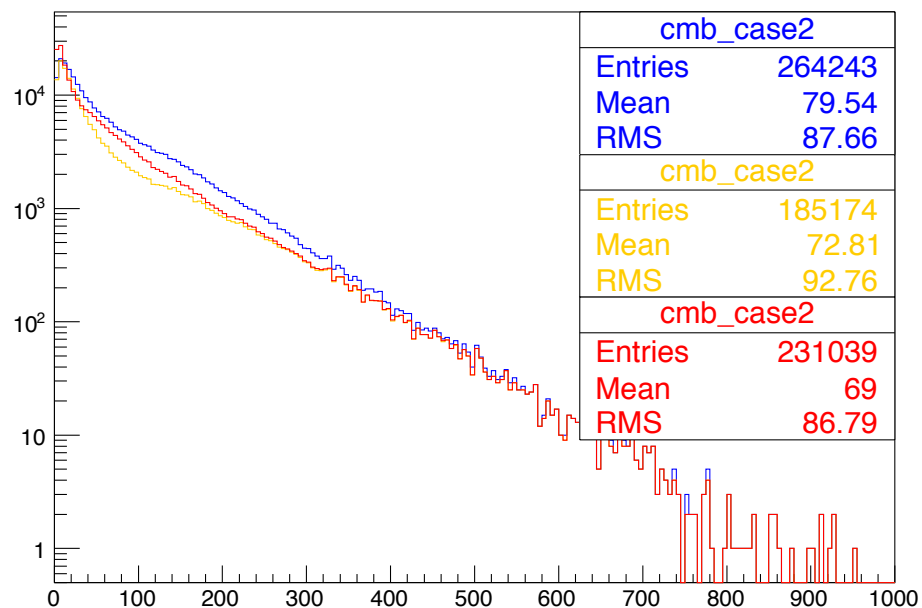
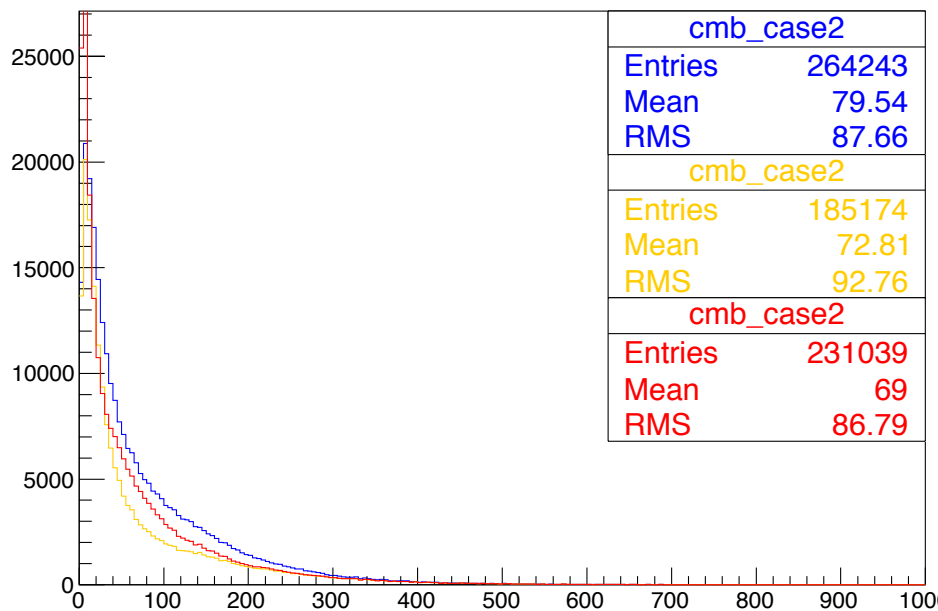
- **Scenario1**: e.g.) C-B $\rightarrow$ A-B, C-E $\rightarrow$ A-E
- **Scenario2**: e.g.) C-B $\rightarrow$ C-E, C-E $\rightarrow$ C-B
- **Scenario3**: e.g.) C-B $\rightarrow$ C-E, C-E $\rightarrow$ C-B



Case2

ATCA Fabric

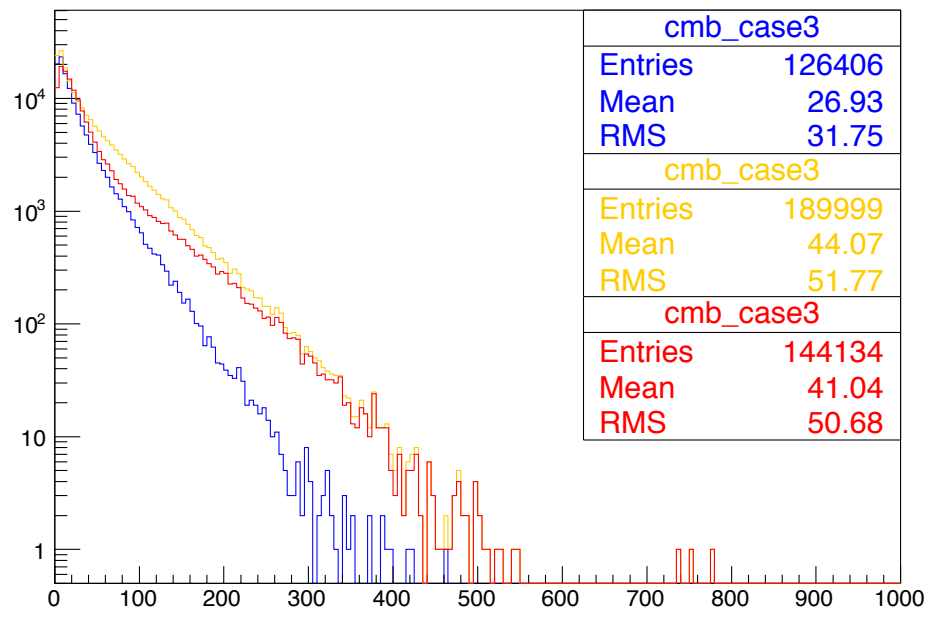
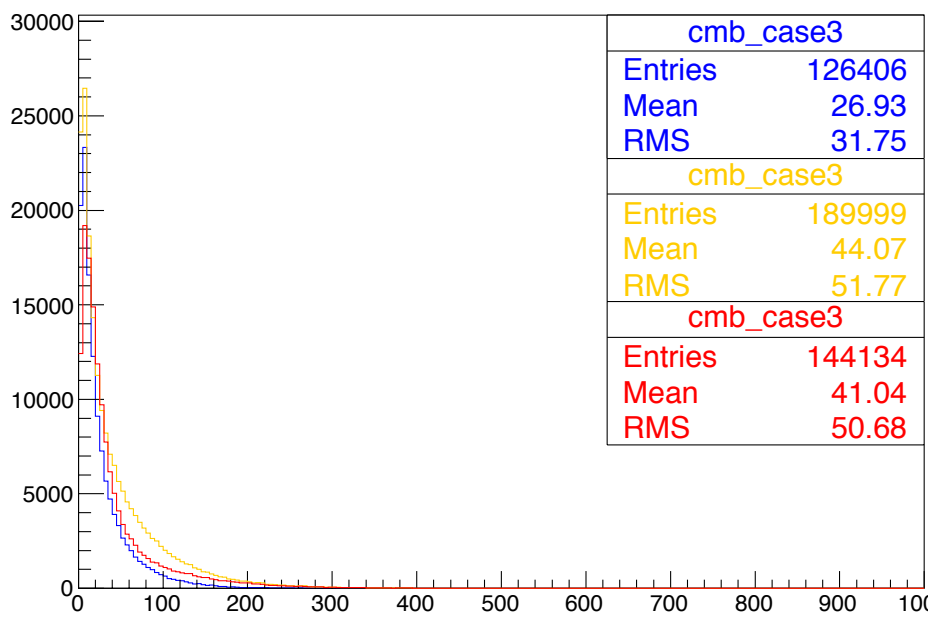
- **Scenario1**: e.g.) C-B $\rightarrow$ C-E, C-B $\rightarrow$ C-E
- **Scenario2**: e.g.) C-B $\rightarrow$ A-E, C-E $\rightarrow$ A-B
- **Scenario3**: e.g.) C-B $\rightarrow$ A-B, C-E $\rightarrow$ A-E



Case3

ATCA Fabric + Inter-FPGA

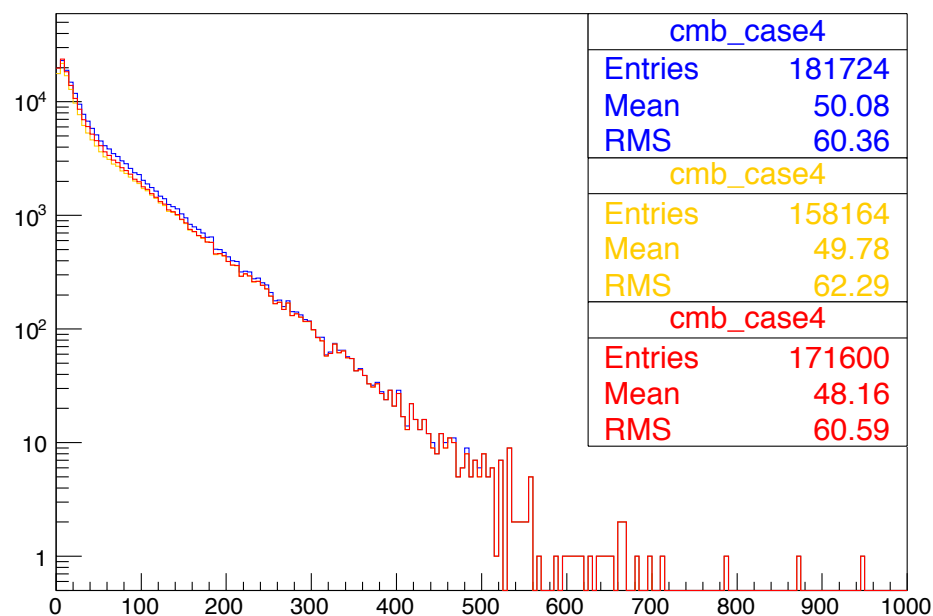
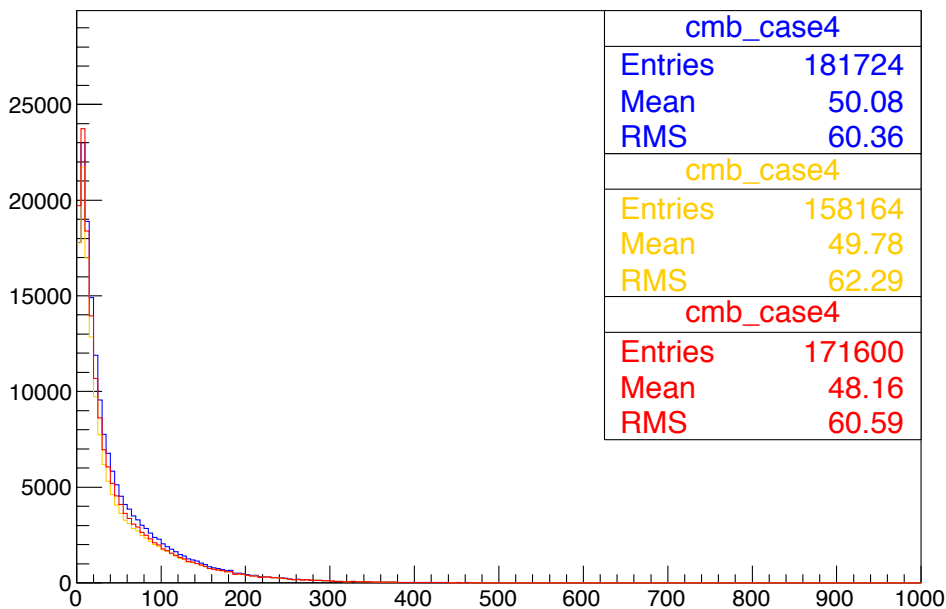
- **Scenario1**: e.g.) C-B $\rightarrow$ A-B, C-E $\rightarrow$ A-E
- **Scenario2**: e.g.) C-B $\rightarrow$ A-B, C-E $\rightarrow$ A-E
- **Scenario3**: e.g.) C-B $\rightarrow$ A-E, C-E $\rightarrow$ A-B



Case4

Inter-crate

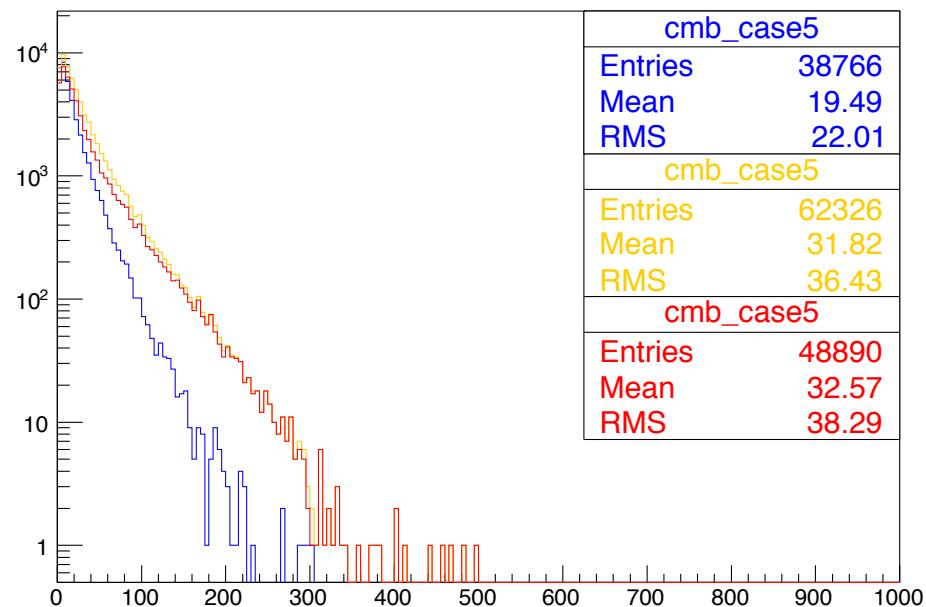
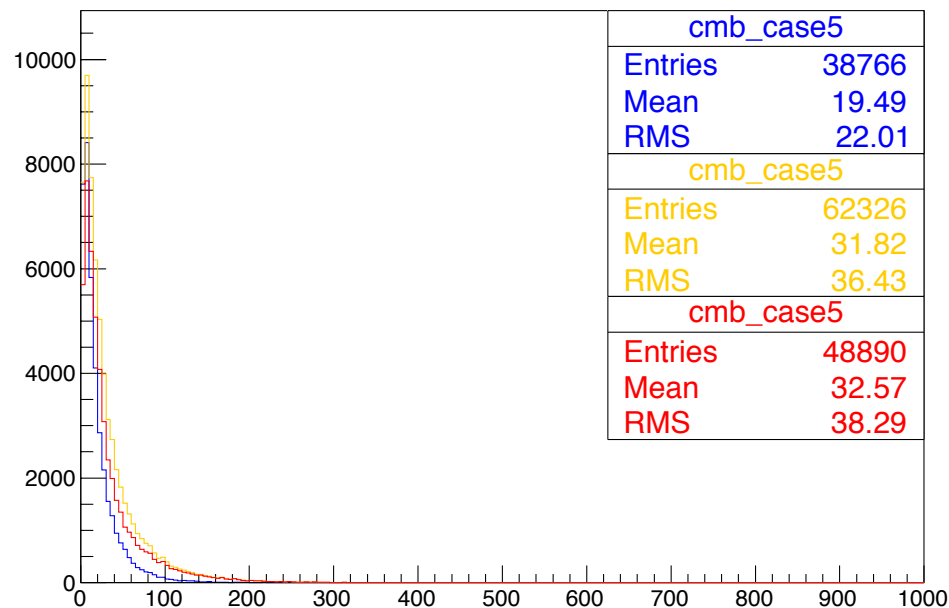
- **Scenario1**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-B}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-E}$
- **Scenario2**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-B}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-E}$
- **Scenario3**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-B}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-B}$



Case5

Inter-crate + Inter-FPGA

- **Scenario1**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-B}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-E}$
- **Scenario2**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-E}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-B}$
- **Scenario3**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-E}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-E}$

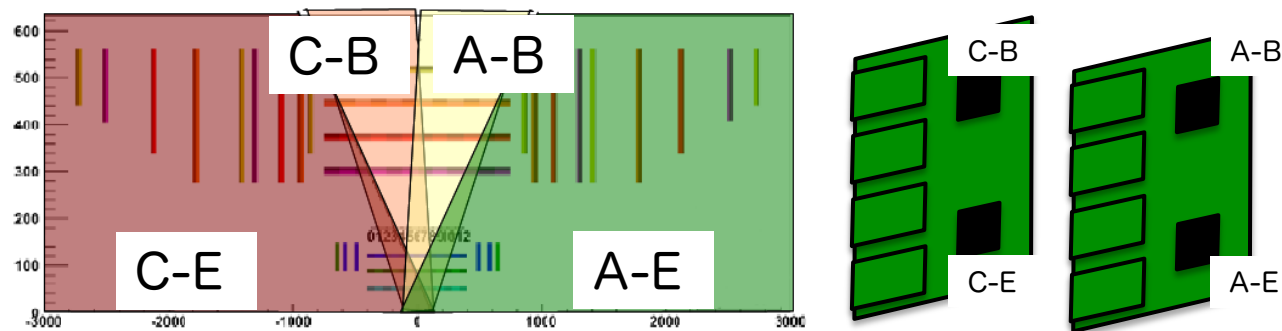


With different Luminosity

Used dataset for the study

- Run 182766, LumiBlock 226 with #pileup = 7.3
- Run 191426, LumiBlock 563 with #pileup = 10.2
- Run 201556, LumiBlock 450 with #pileup = 23.1

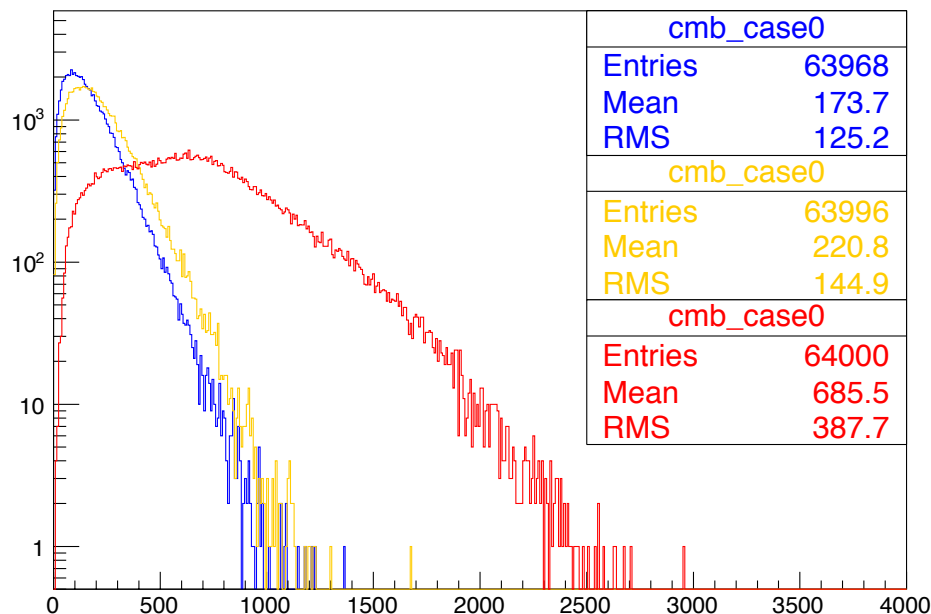
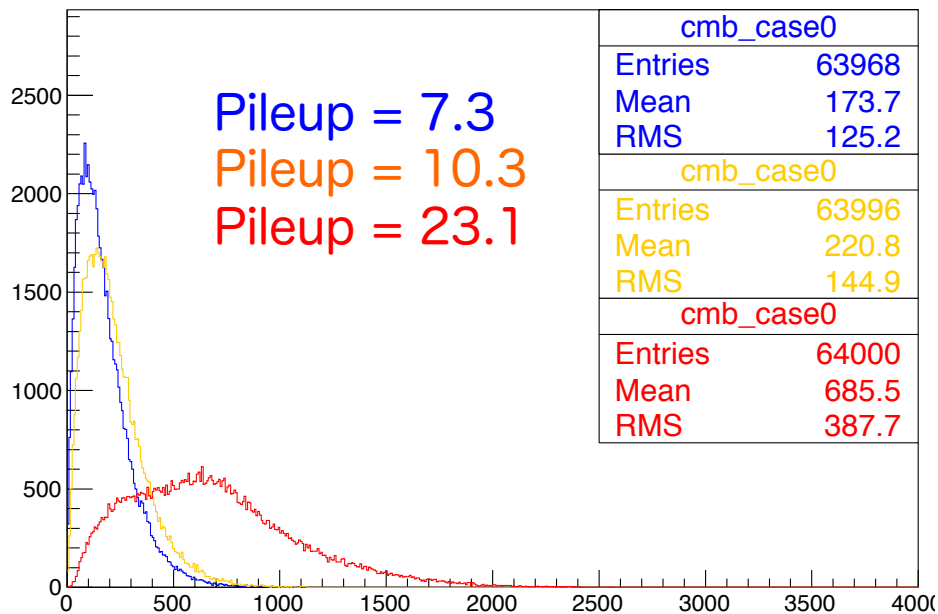
Board alignment



Case0

Directly go to AUX

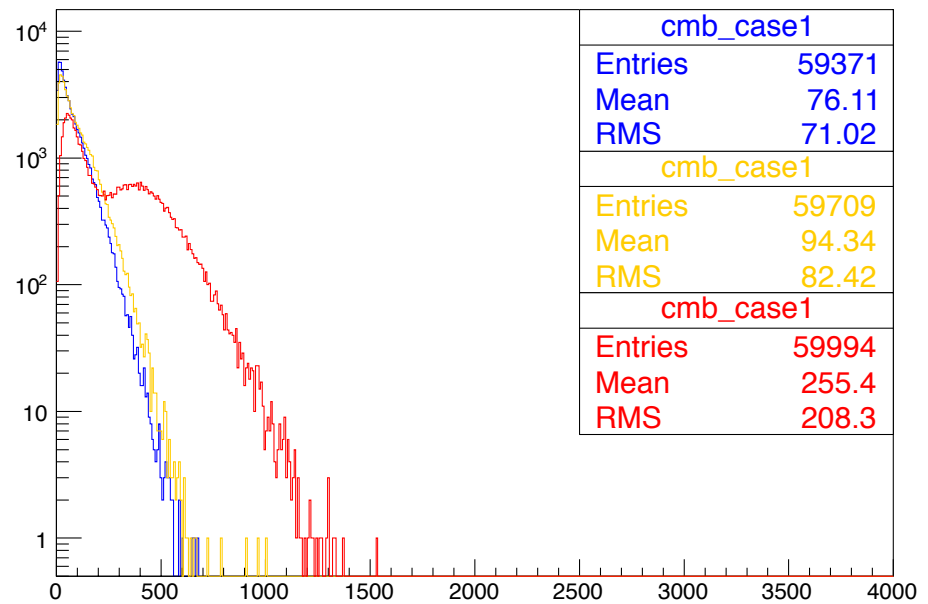
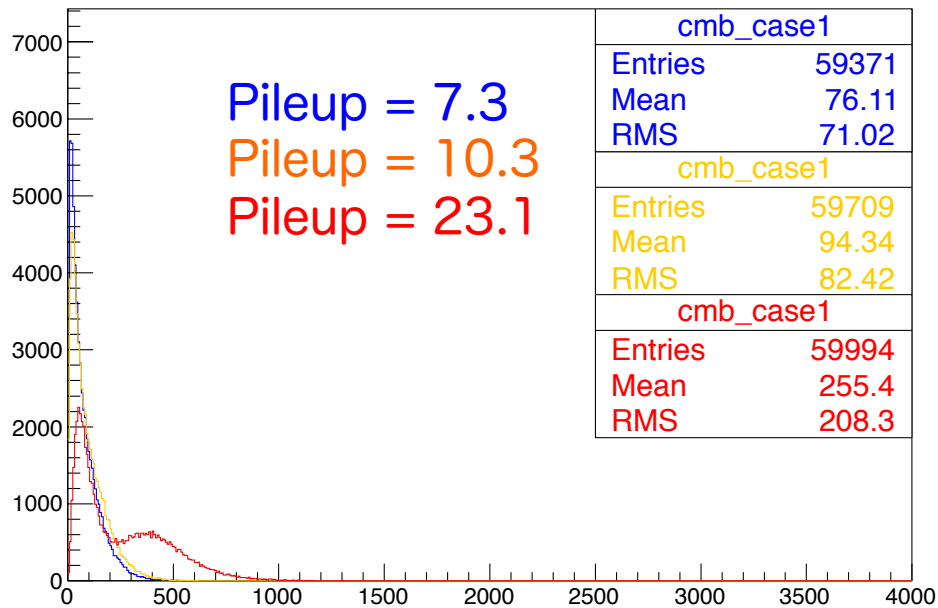
- **Scenario3**: e.g.) C-B $\rightarrow$ C-B, C-E $\rightarrow$ C-E



Case1

Inter-FPGA communication

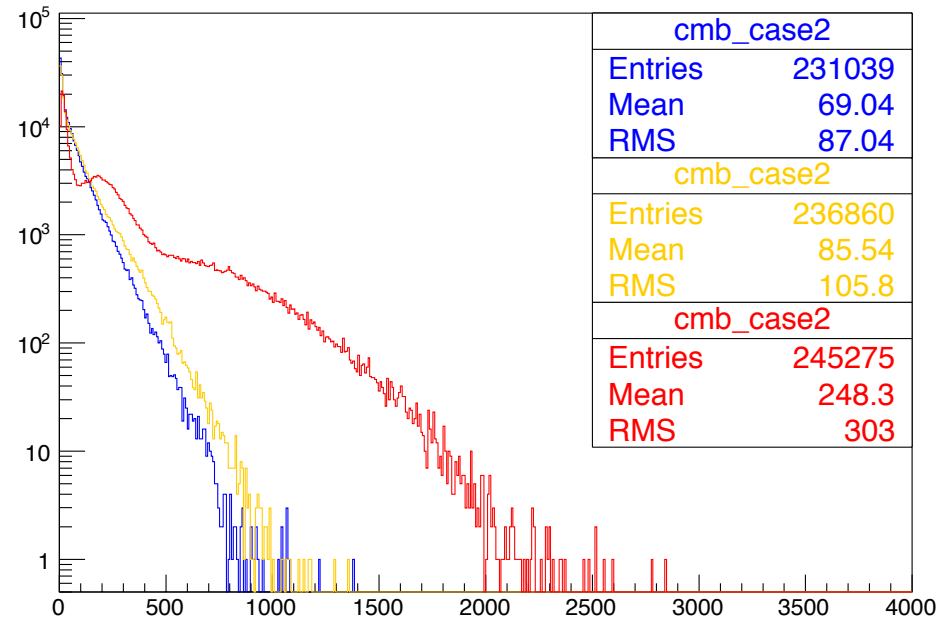
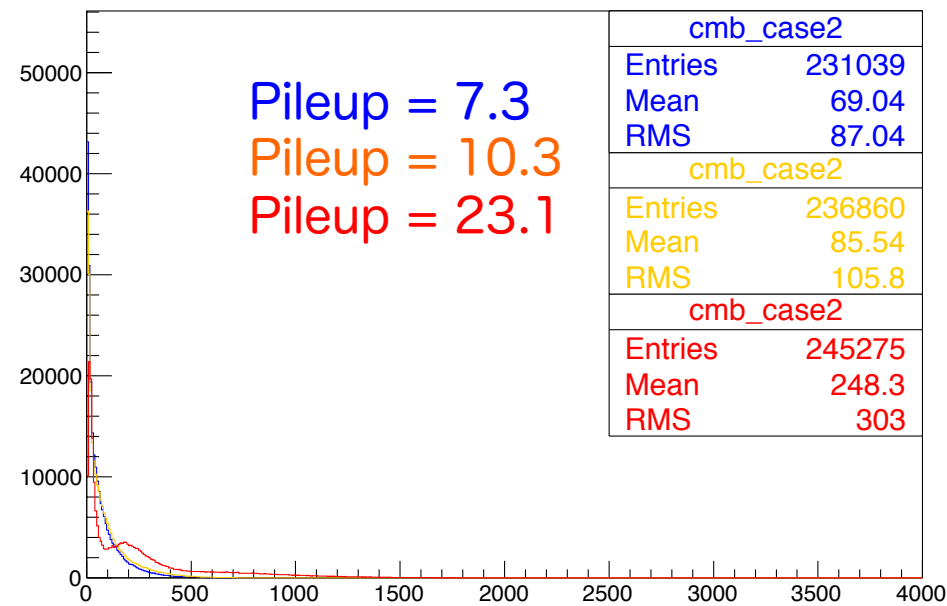
- **Scenario3**: e.g.) C-B $\rightarrow$ C-E, C-E $\rightarrow$ C-B



Case2

ATCA fabric

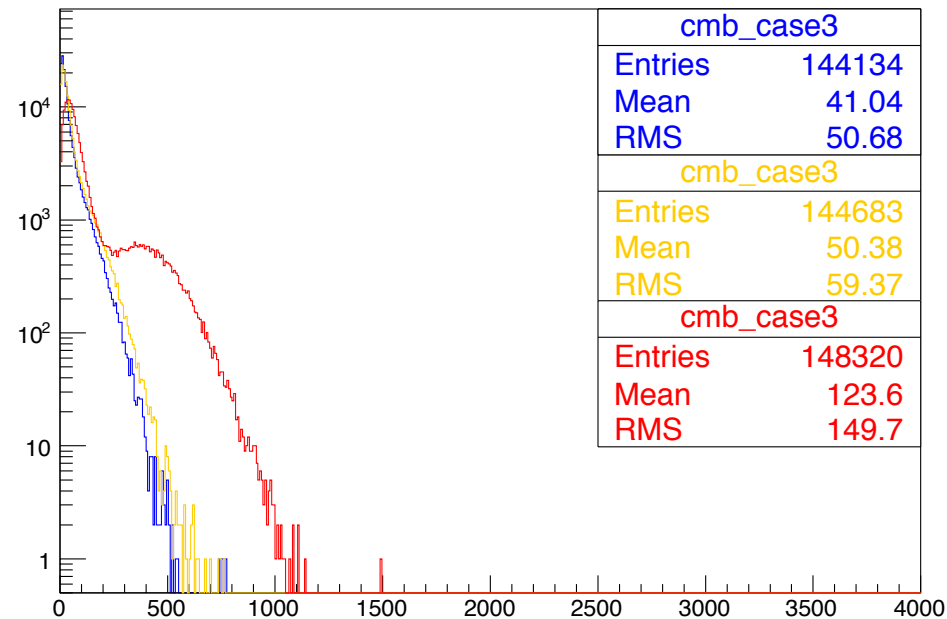
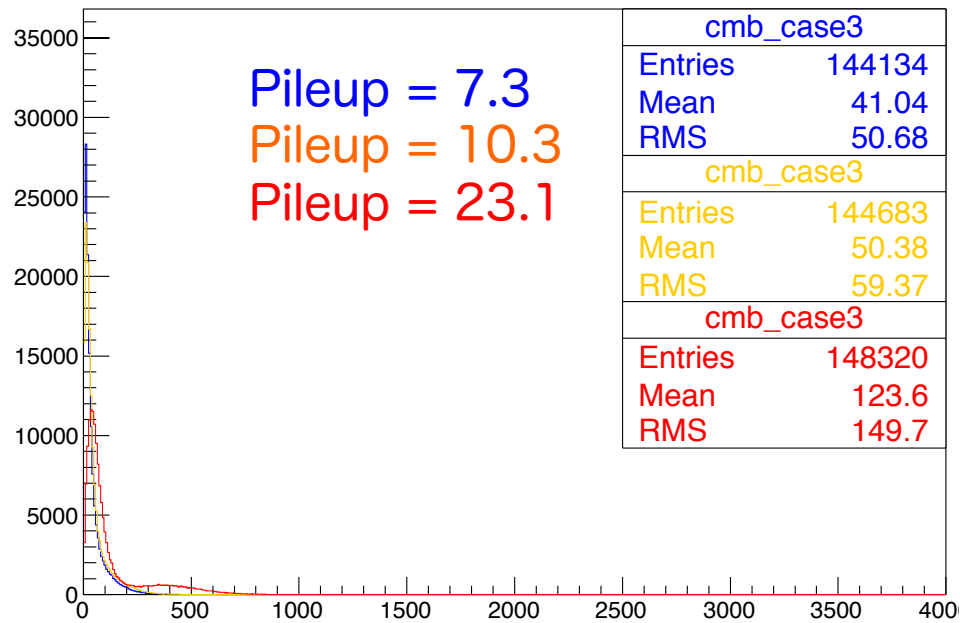
- **Scenario3**: e.g.) C-B → A-B, C-E → A-E



Case3

ATCA fabric + Inter-FPGA

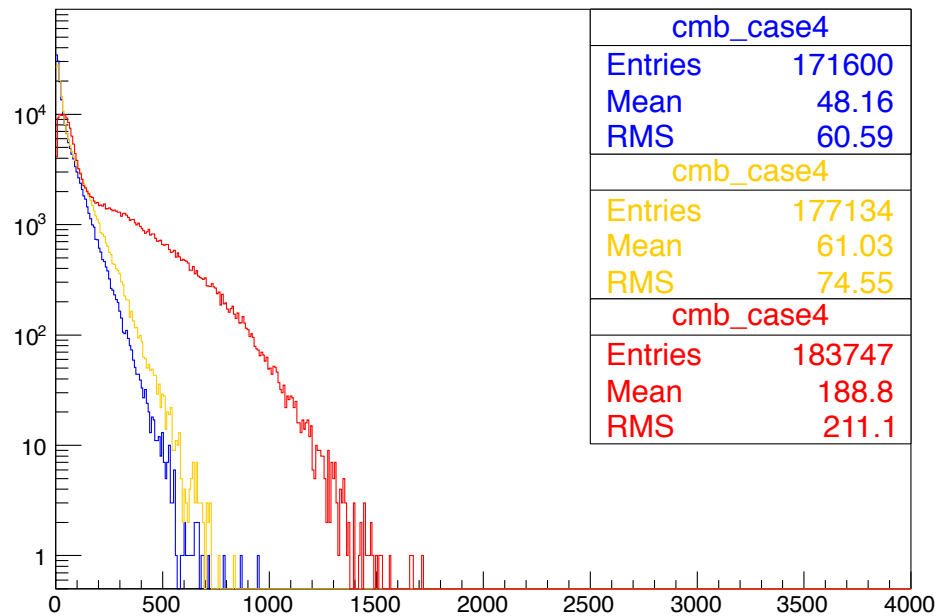
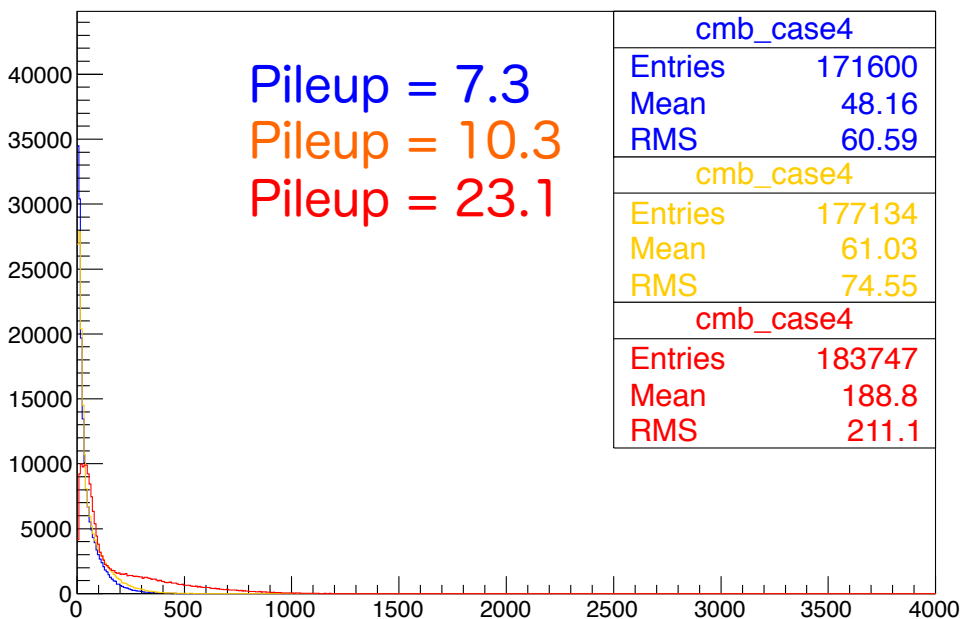
- **Scenario3**: e.g.) C-B $\rightarrow$ A-E, C-E $\rightarrow$ A-B



Case4

Inter-crate

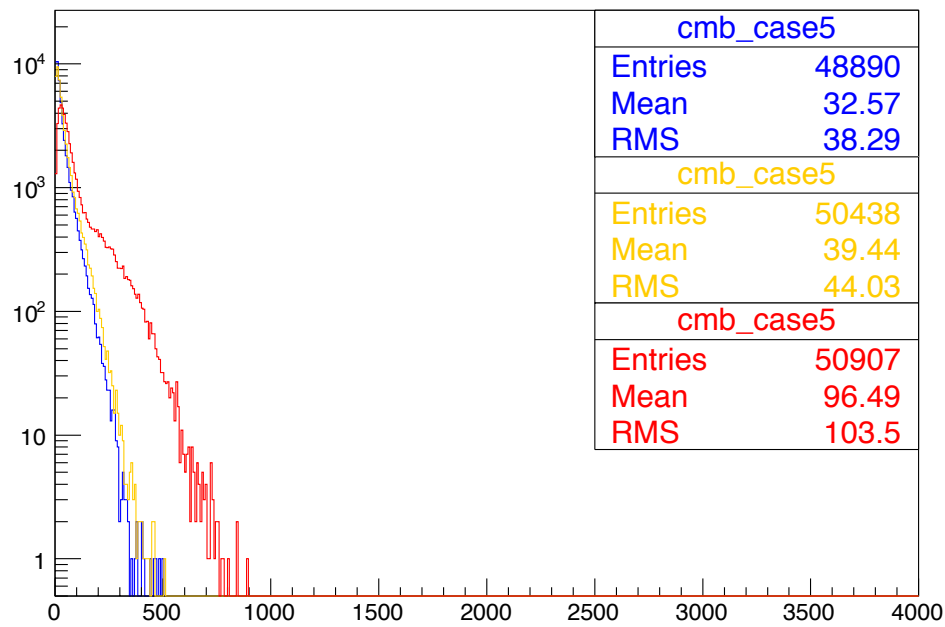
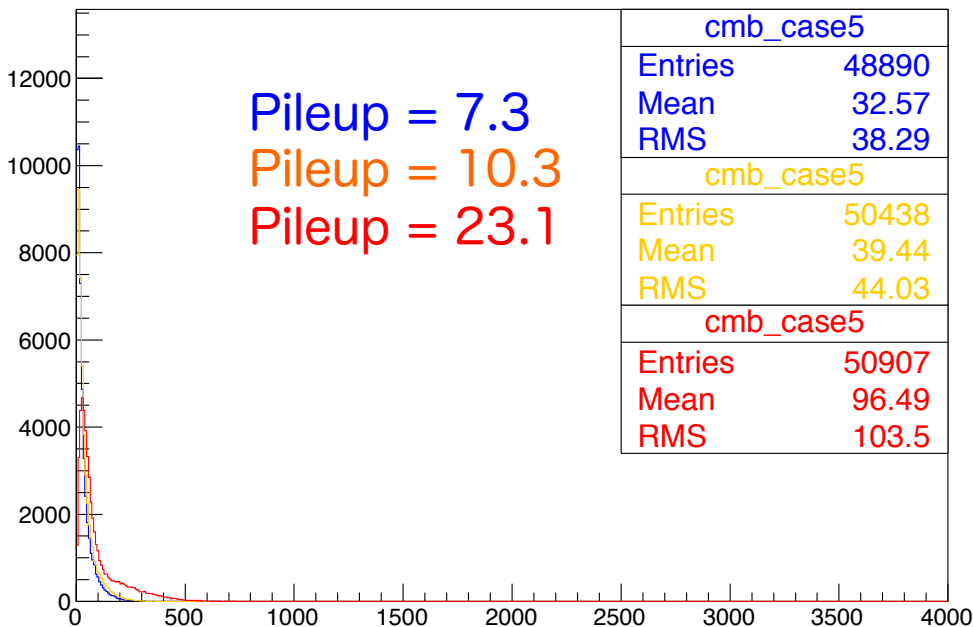
- **Scenario3**: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-B}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-B}$



Case5

Inter-crate + Inter-FPGA

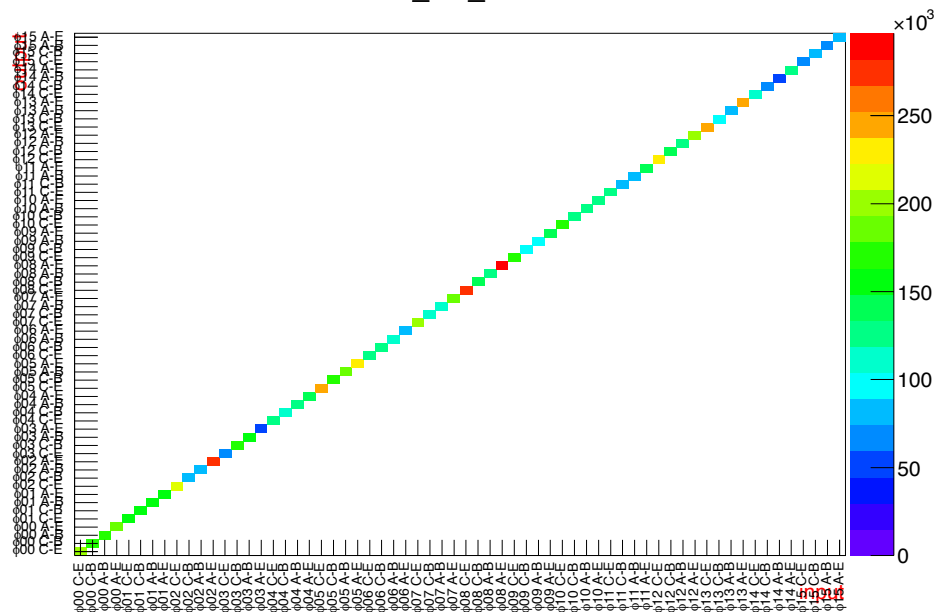
- Scenario3: e.g.) $\phi 0\text{-C-B} \rightarrow \phi 4\text{-C-E}$, $\phi 0\text{-C-B} \rightarrow \phi 4\text{-A-E}$



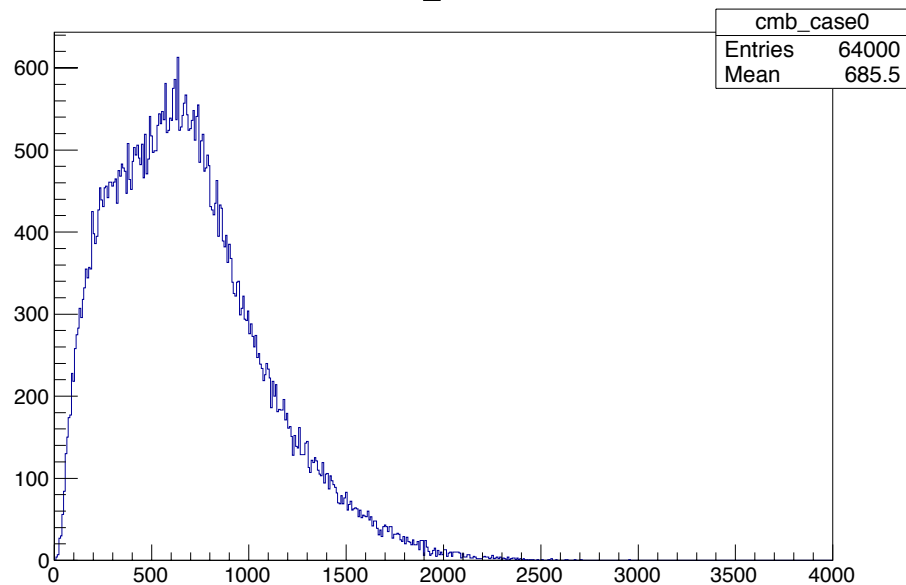
High luminosity runs

Case0

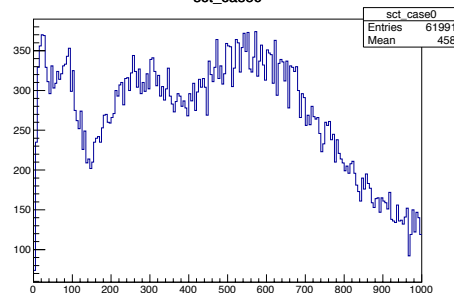
cmb_2D_case0



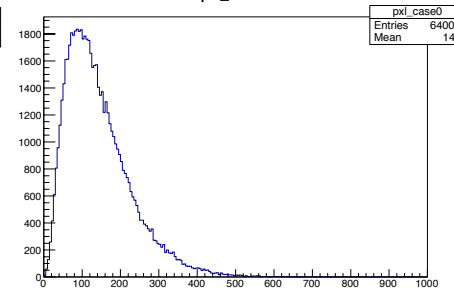
cmb_case0



sct_case0

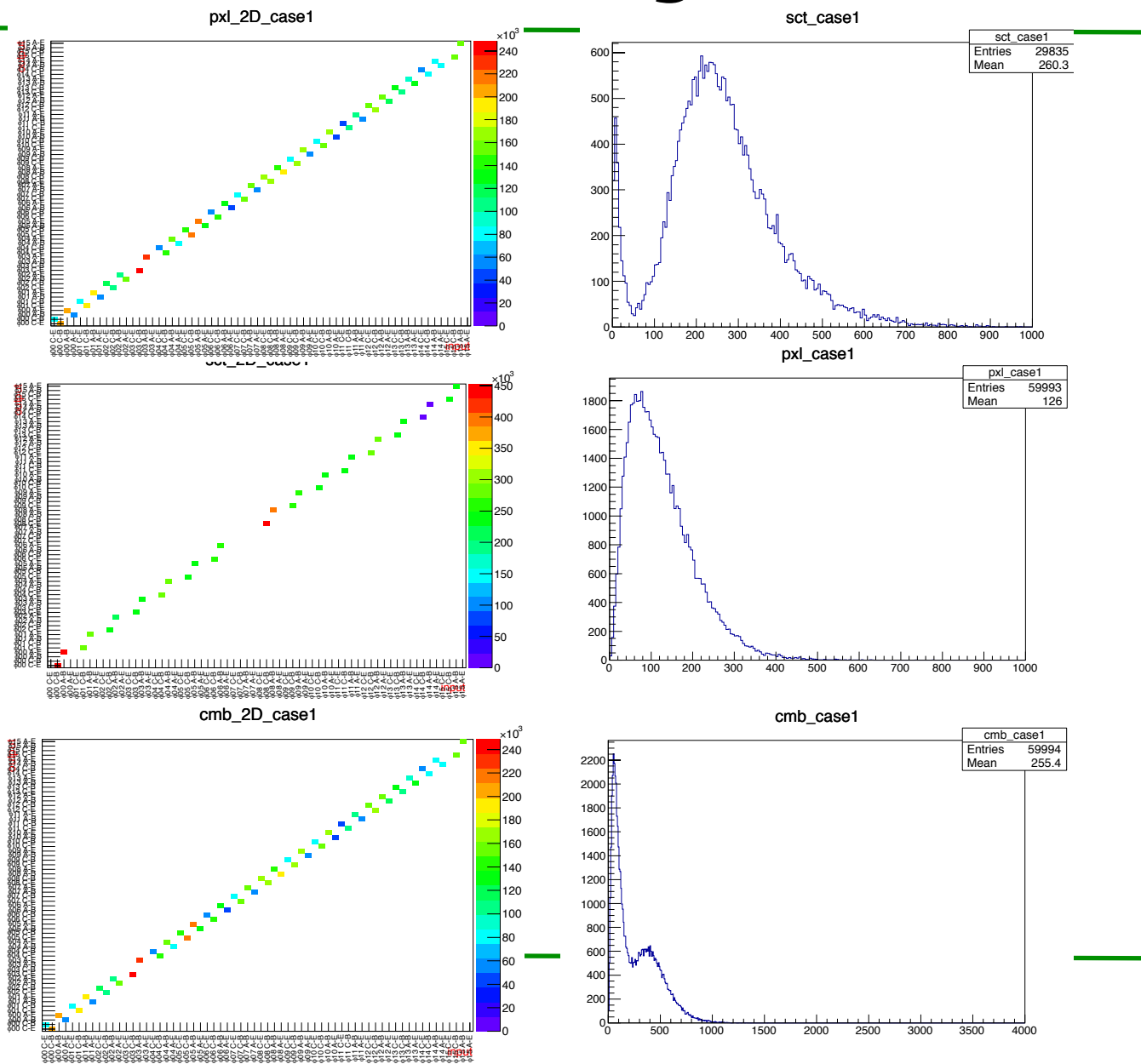


pxl_case0



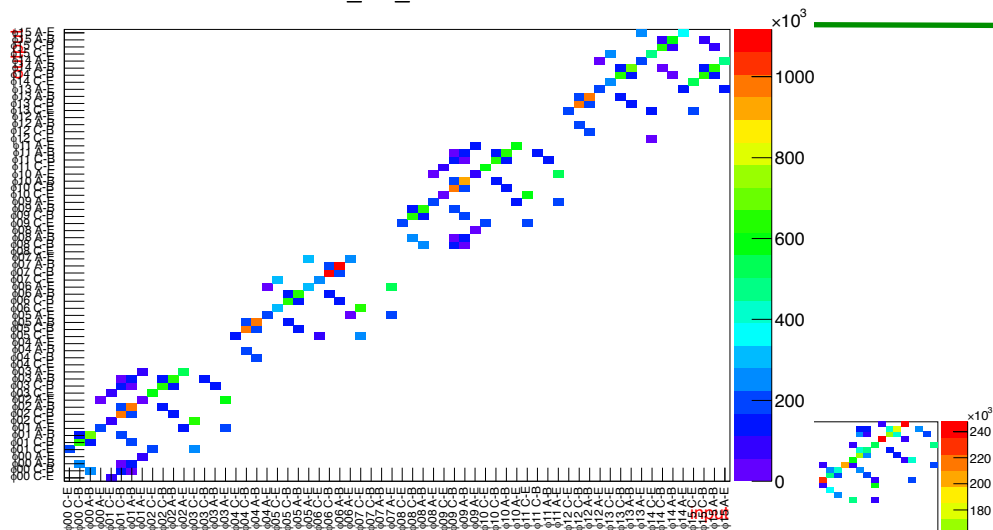
High luminosity runs

Case 1

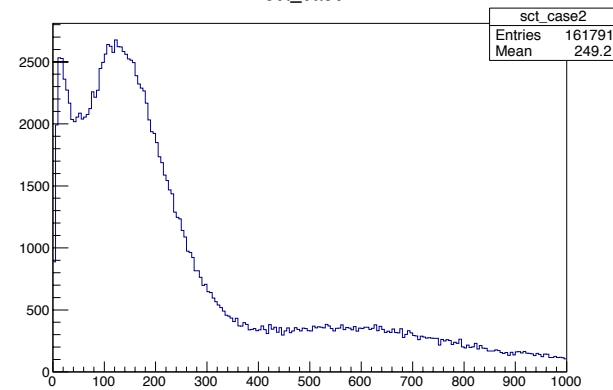


High luminosity runs

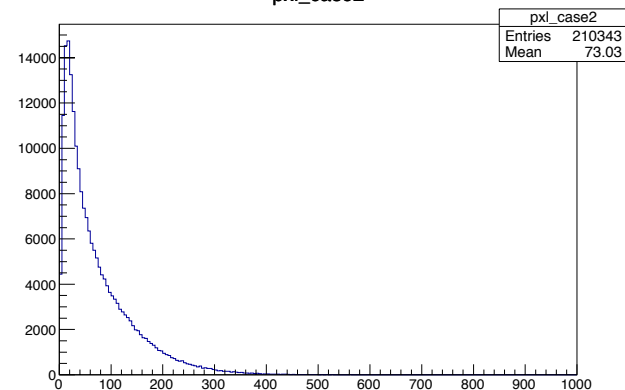
sct_2D_case2



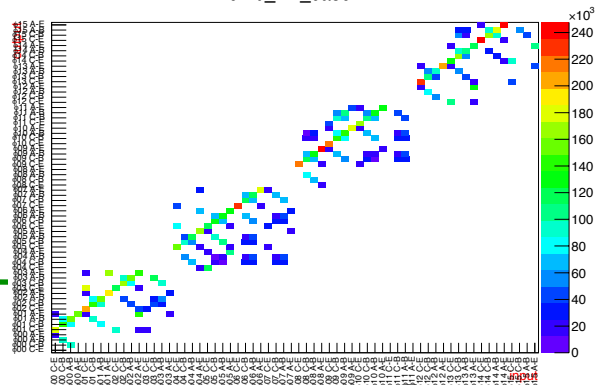
sct_case2



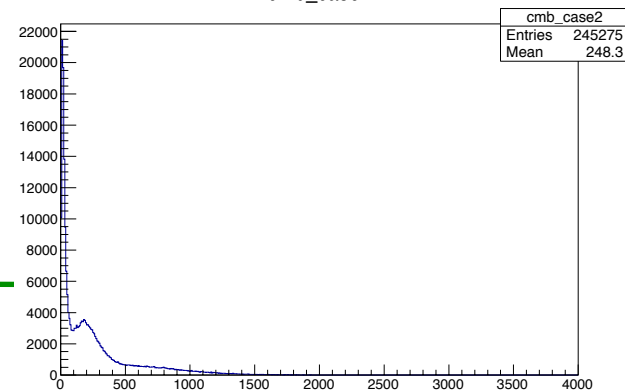
pxl_case2



cmb_2D_case2

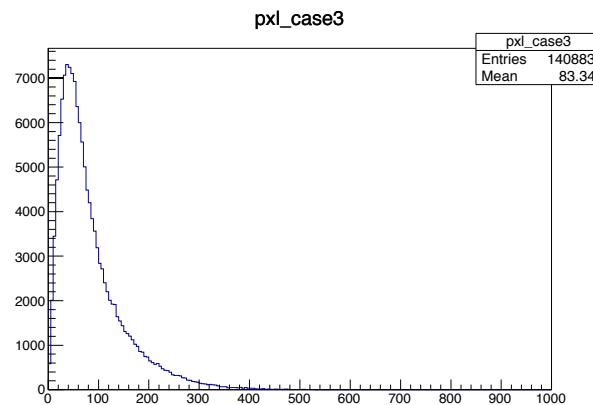
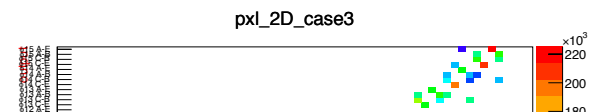
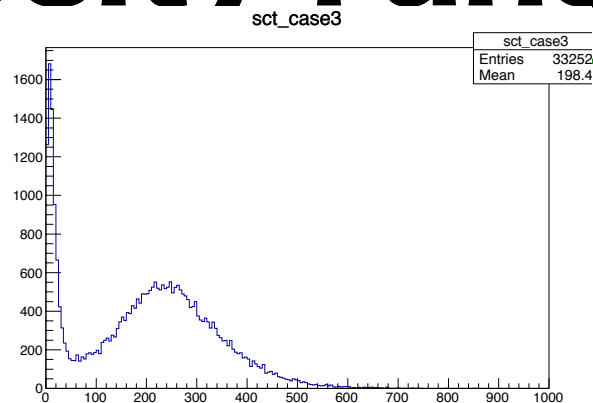
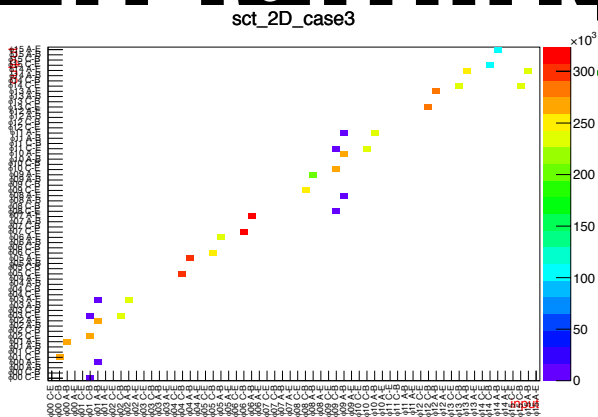


cmb_case2

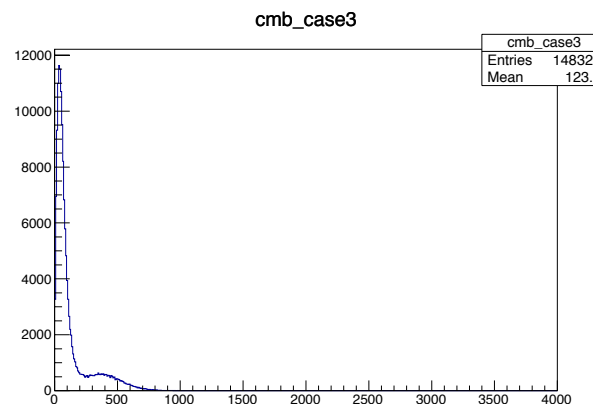
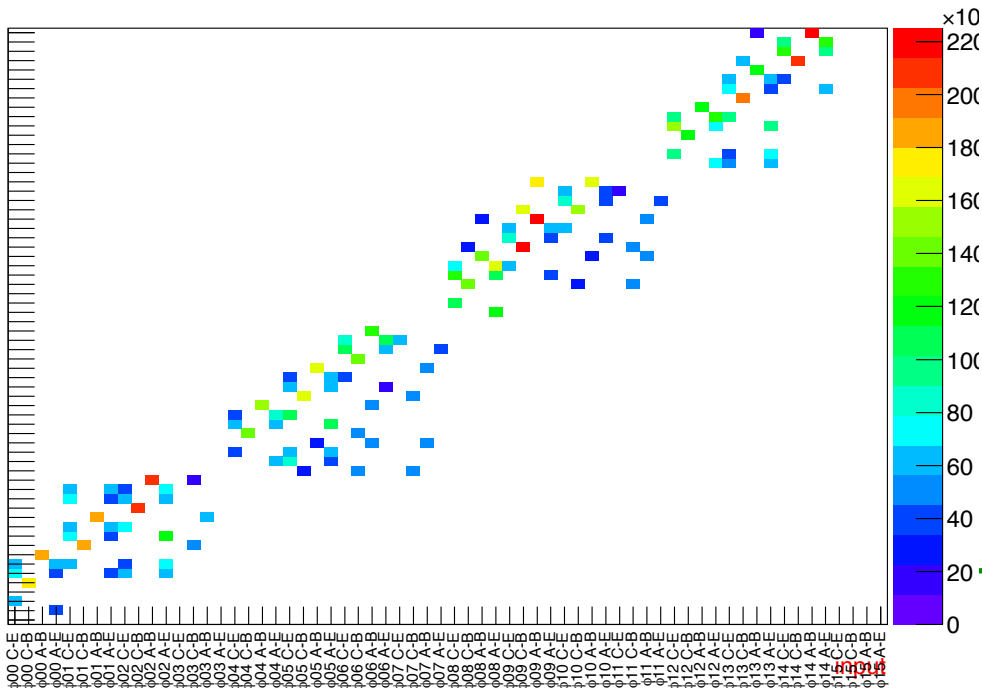


High luminosity runs

Case3

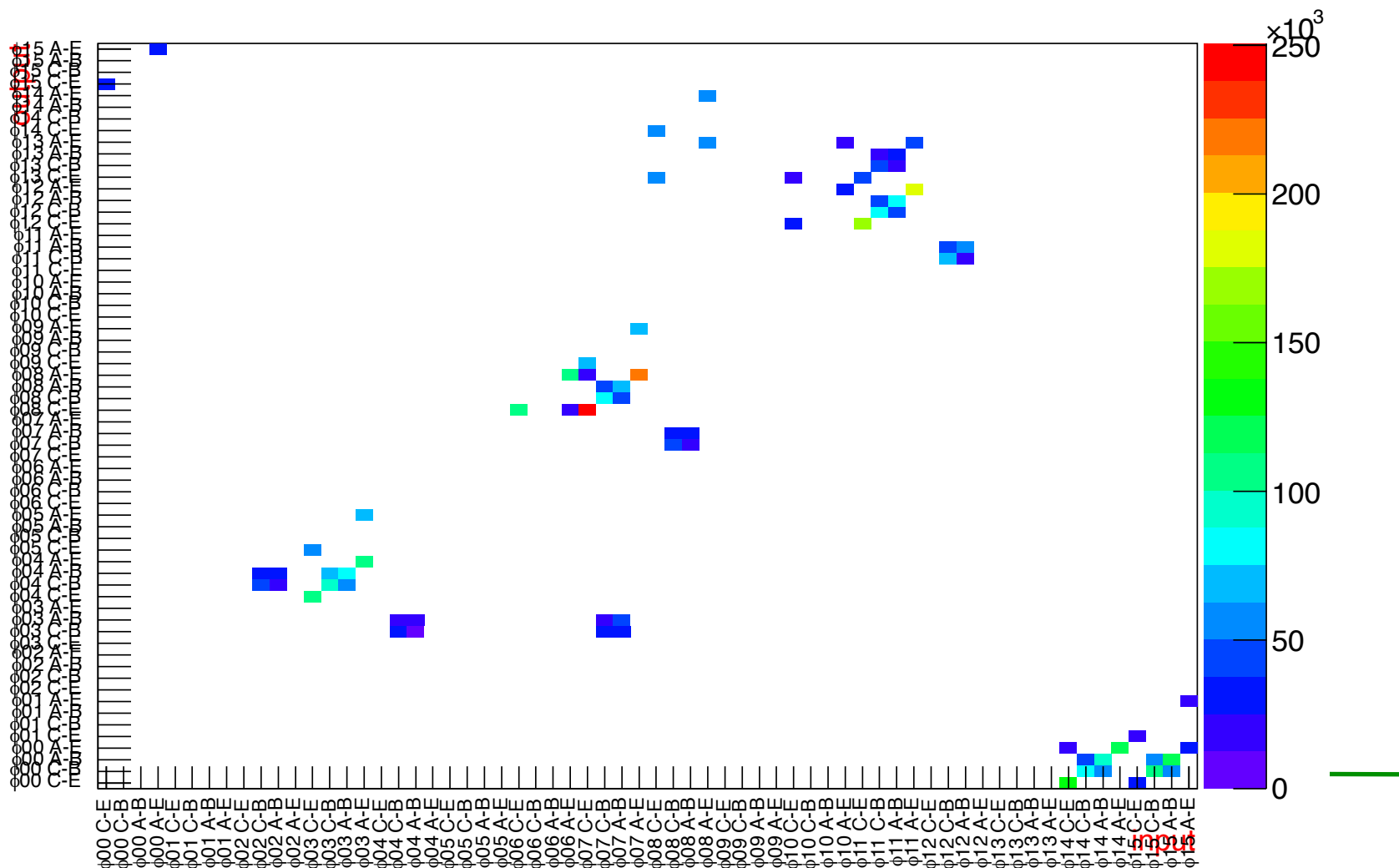
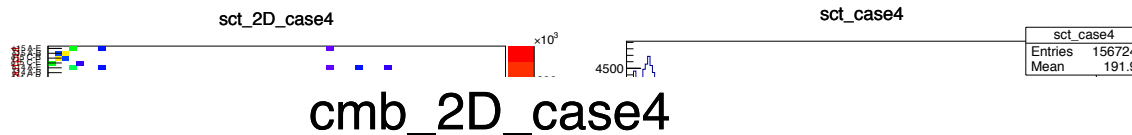


cmb_2D_case3



High luminosity runs

Case4



High luminosity runs

Case 5

