
Data volume summary

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Data

- data12 with 8 TeV
 - Run 201556 LB: 450 $\langle\mu\rangle = 23.1$
 - Run 201556 LB: 526 $\langle\mu\rangle = 20.0$
 - Run 201556 LB: 670 $\langle\mu\rangle = 16.0$
 - Run 201556 LB: 774 $\langle\mu\rangle = 14.0$
 - Run 201556 LB: 928 $\langle\mu\rangle = 12.0$
 - Run 201556 LB: 1039 $\langle\mu\rangle = 10.7$
 - data11 with 7TeV
 - Run 191426 LB:563 $\langle\mu\rangle = 10.2$
 - Run 182766 LB:226 $\langle\mu\rangle = 7.3$
 - Run 167067 LB:159 $\langle\mu\rangle = 3.2$
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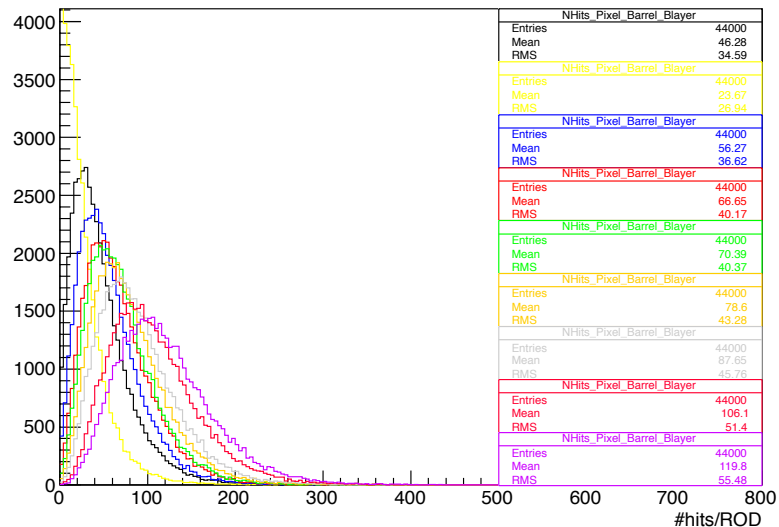
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- The diagram illustrates a multi-shelf system architecture. It features three green server racks (shelves) arranged in a row. Each rack contains multiple horizontal slots, some of which are populated with black square components. A red line connects a yellow star on the leftmost rack to a yellow star on the middle rack, labeled "To AUX Card". A blue line connects a yellow star on the middle rack to a yellow star on the rightmost rack, labeled "ATCA Fabric". An orange line connects a yellow star on the middle rack to a yellow star on the rightmost rack, labeled "Inter-shelf (ATCA Z3 + opt. link)". The rightmost rack is labeled with a question mark "??".

Inter-FPGA

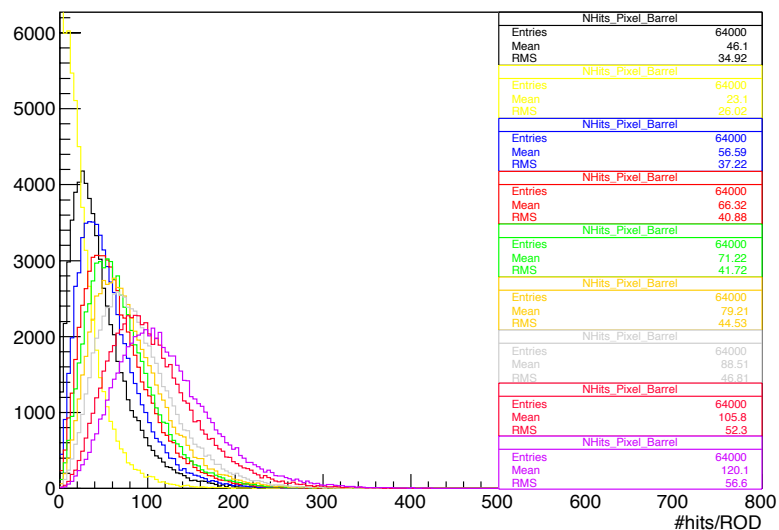
(High speed LVDS on board)

N Pixel Hits/ROD/event

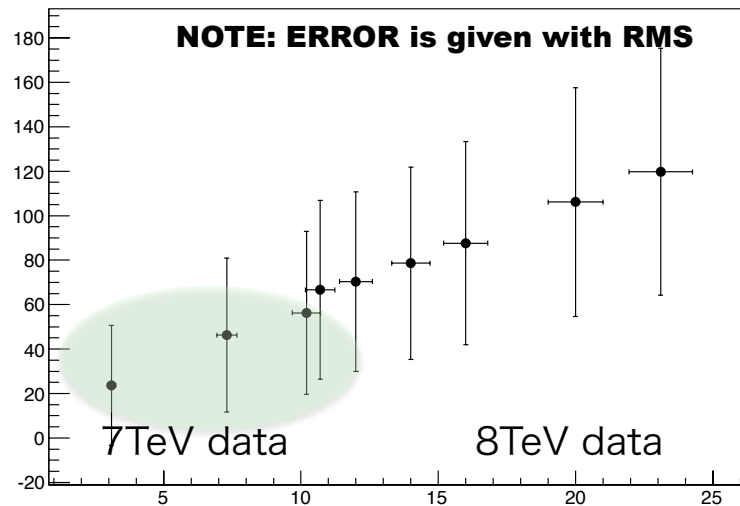
NHits_Pixel_Barrel_Blayer



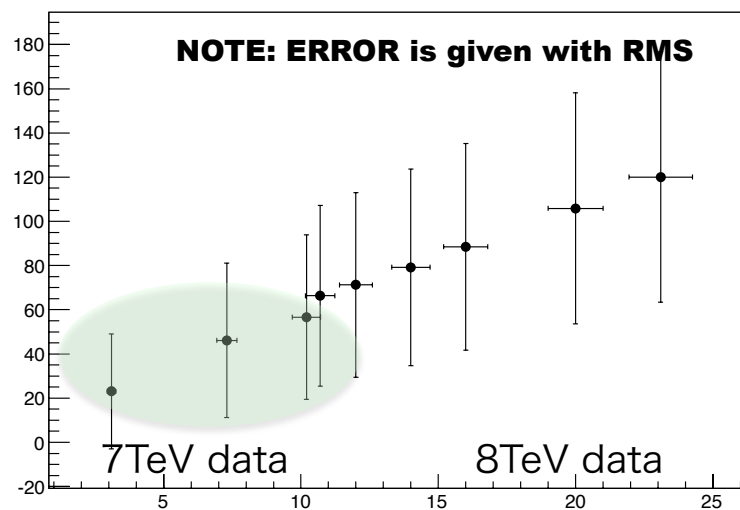
NHits_Pixel_Barrel



NHits_Pixel_Barrel_Blayer

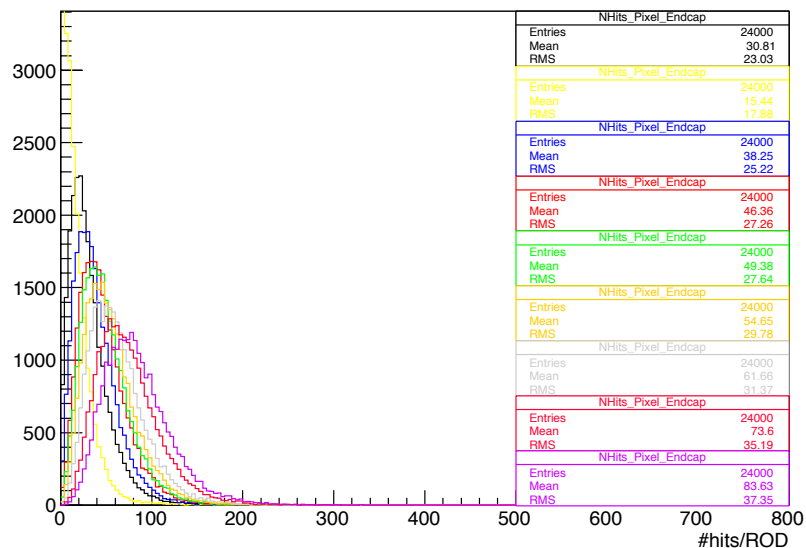


NHits_Pixel_Barrel

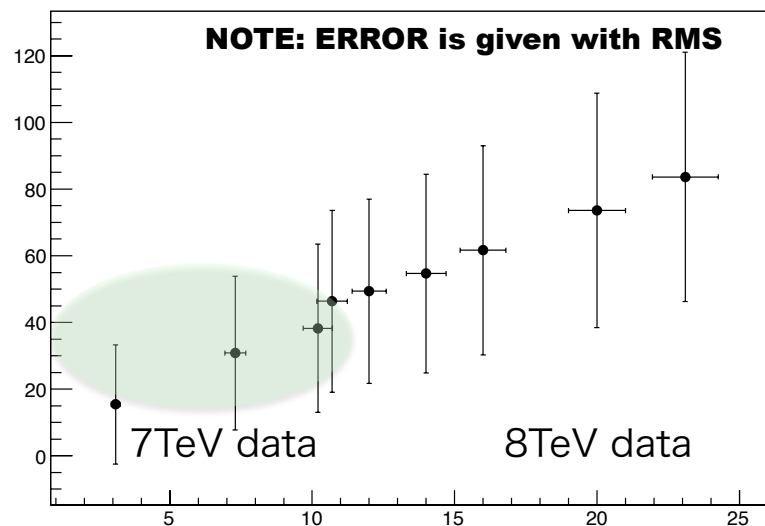


N Pixel Hits/ROD/event

NHits_Pixel_Endcap

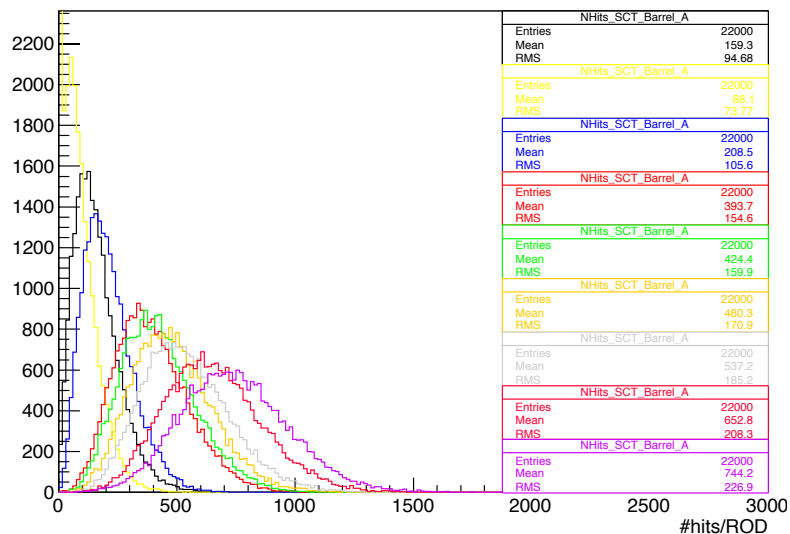


NHits_Pixel_Endcap

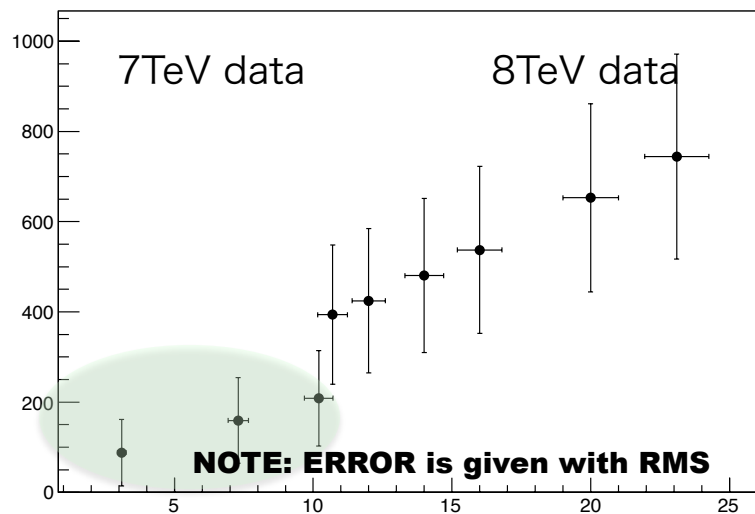


N SCT Hits/ROD/Event

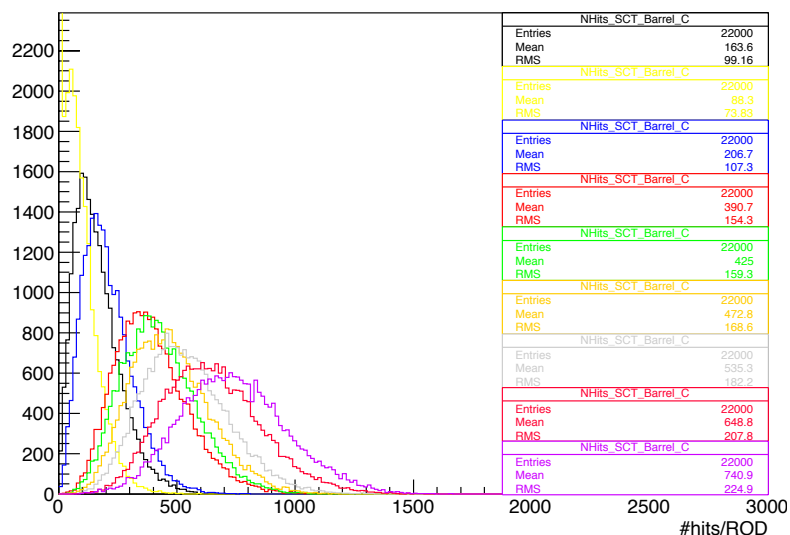
NHits_SCT_Barrel_A



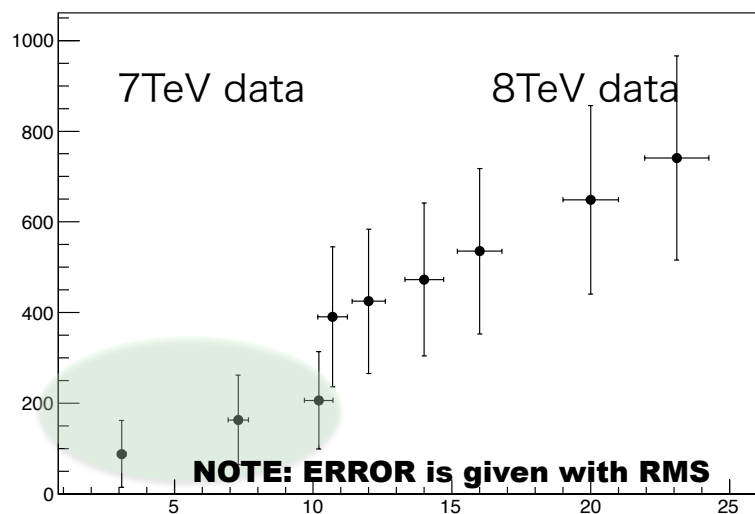
NHits_SCT_Barrel_A



NHits_SCT_Barrel_C

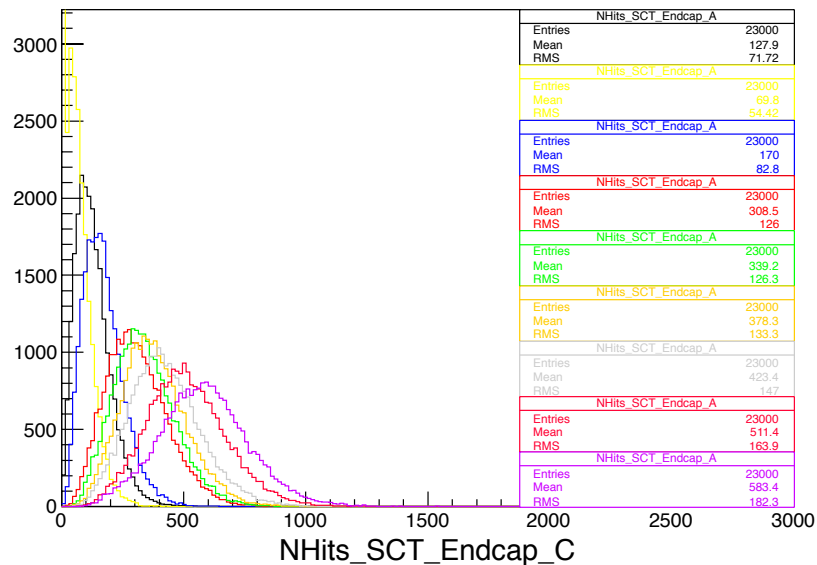


NHits_SCT_Barrel_C

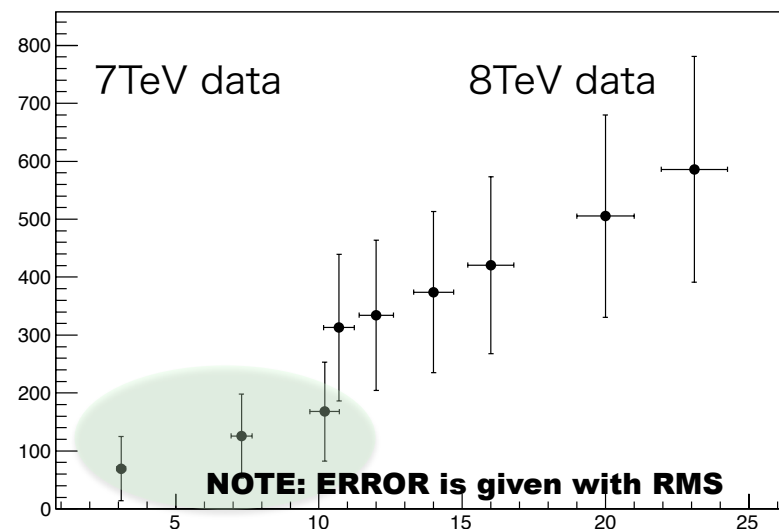
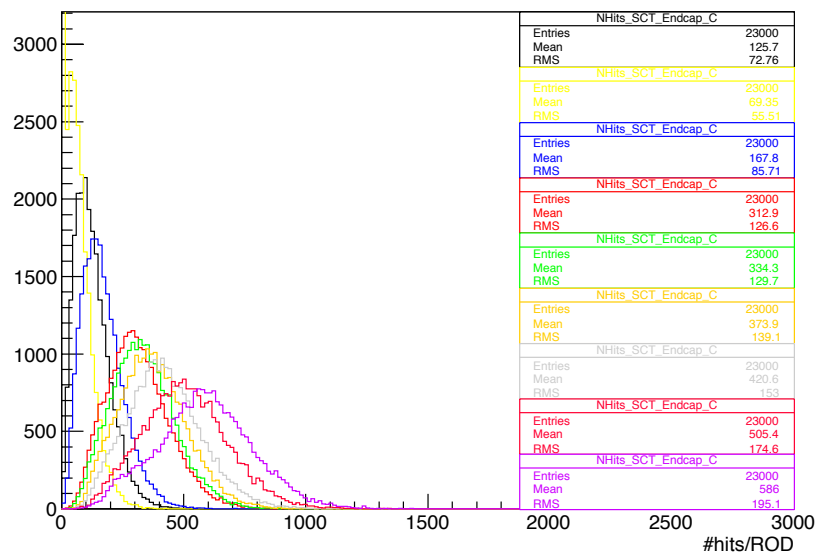
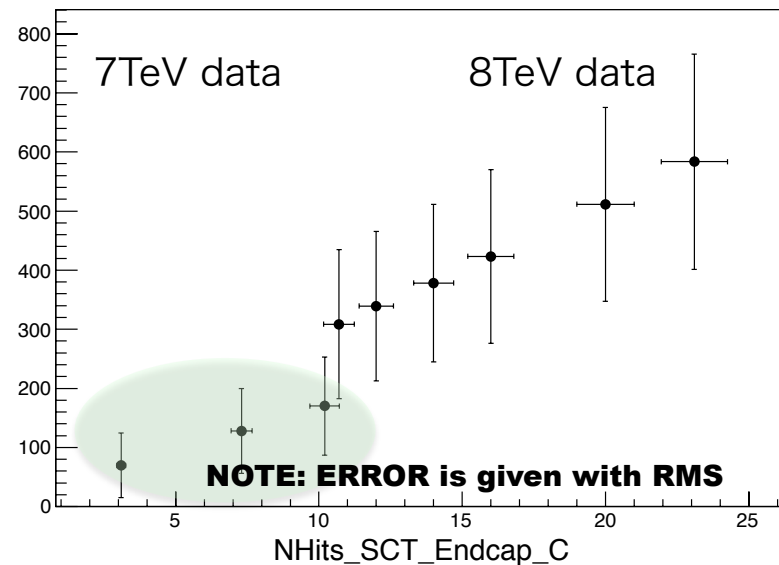


N SCT hits/ROD/Event

NHits_SCT_Endcap_A

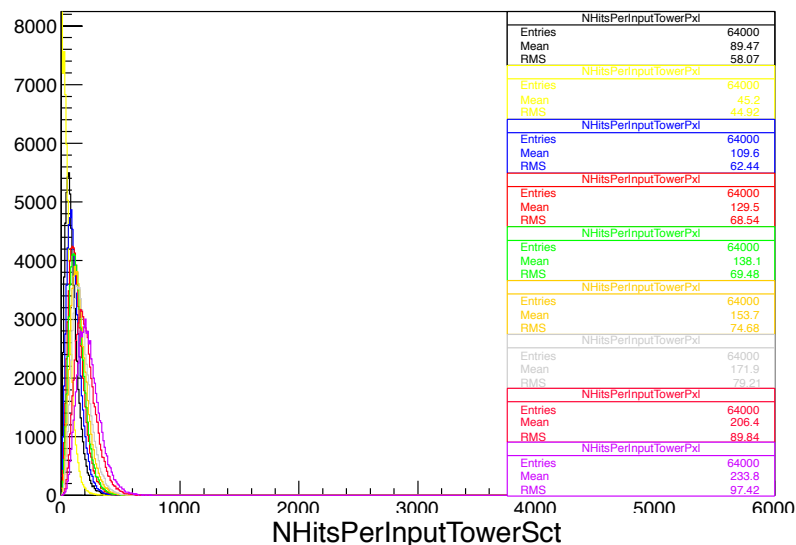


NHits_SCT_Endcap_A

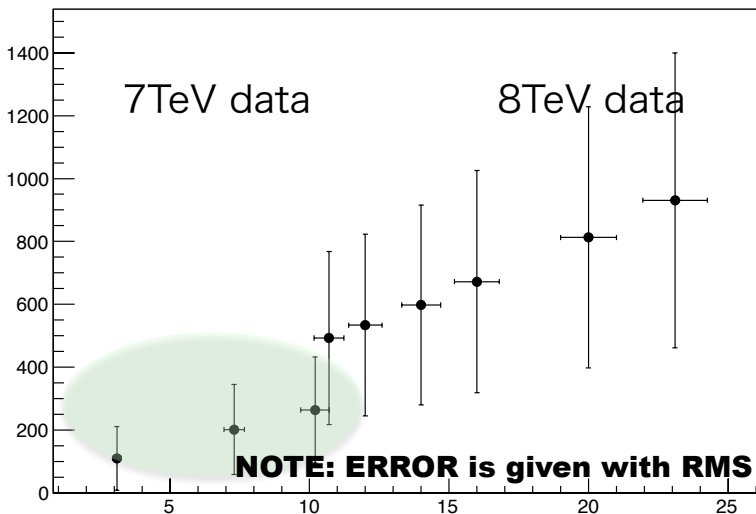
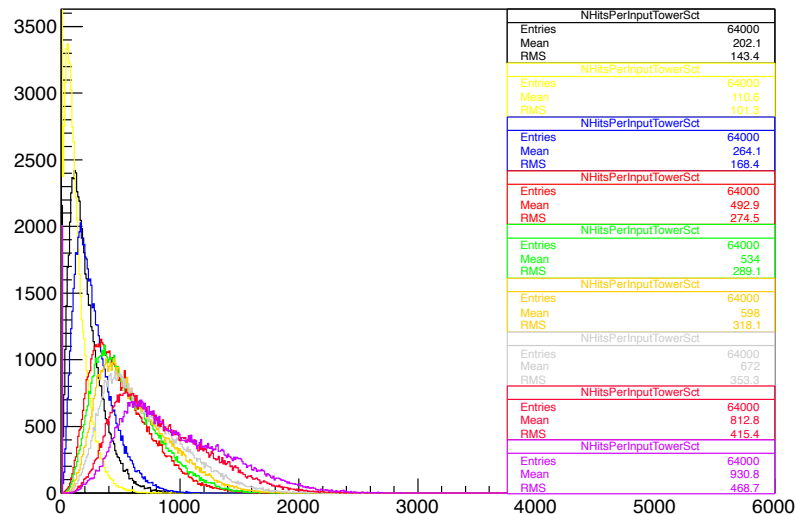
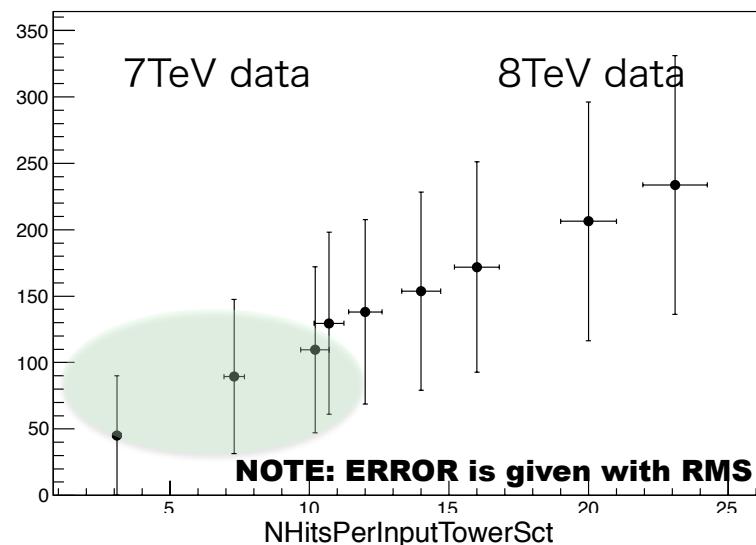


N hits/Tower/event (Input)

NHitsPerInputTowerPxl

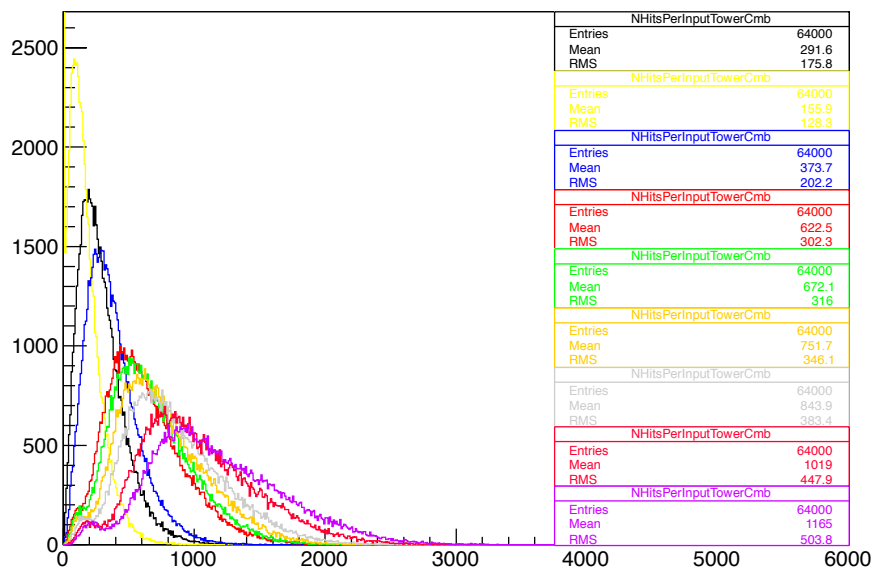


NHitsPerInputTowerPxl

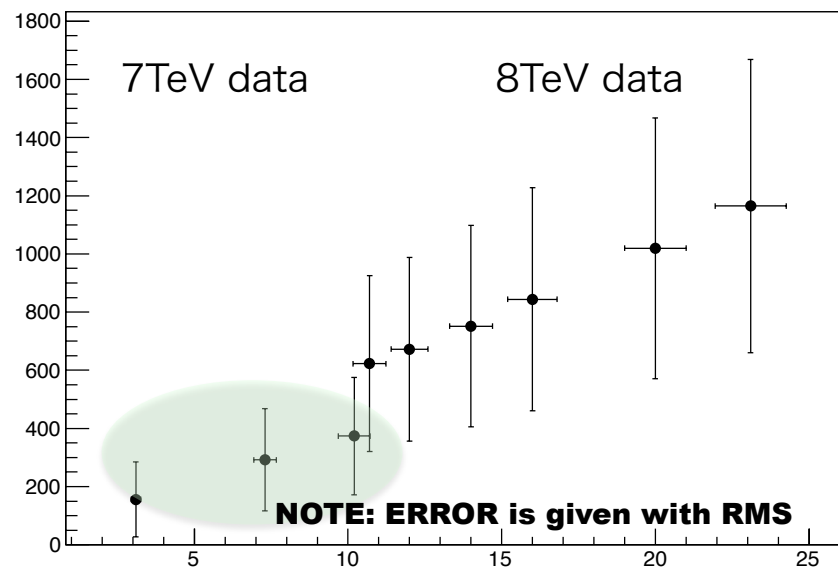


N hits/tower/event (Input)

NHitsPerInputTowerCmb



NHitsPerInputTowerCmb



1,165 hits are input to a FPGA in average with $\langle \mu \rangle = 23$

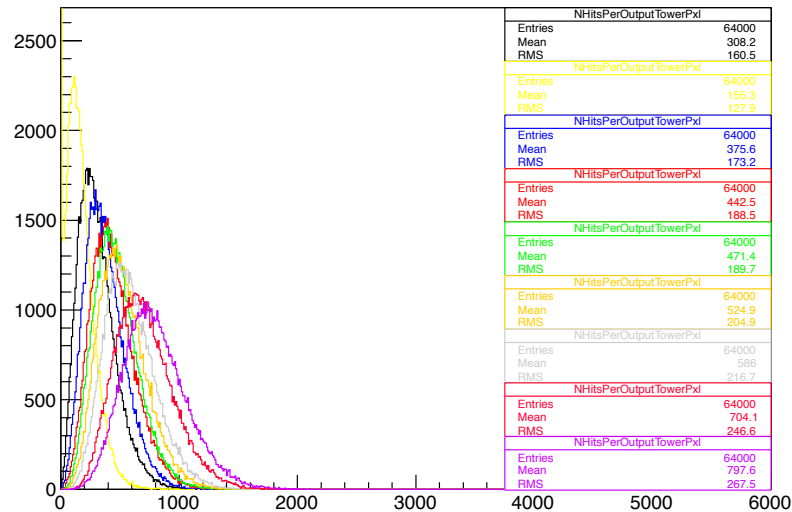
NOTE:

- A ROD cover 1.9 Pixel ROD & 1.4 SCT ROD in average

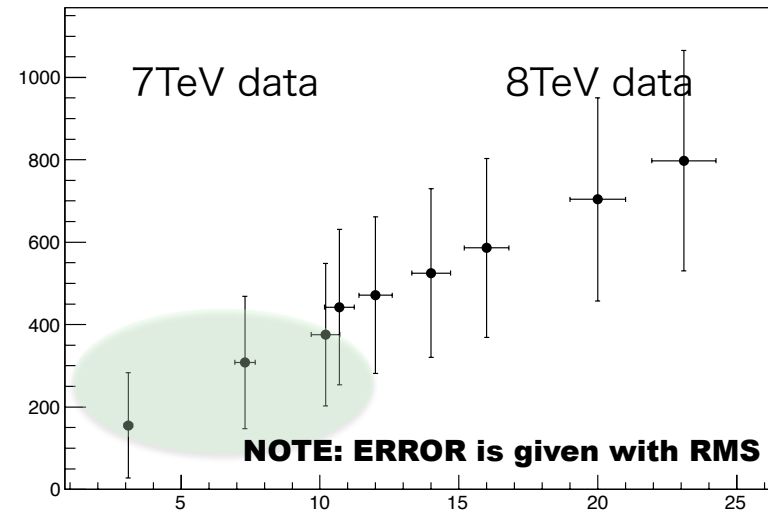
N hits/tower/event (Output)

10

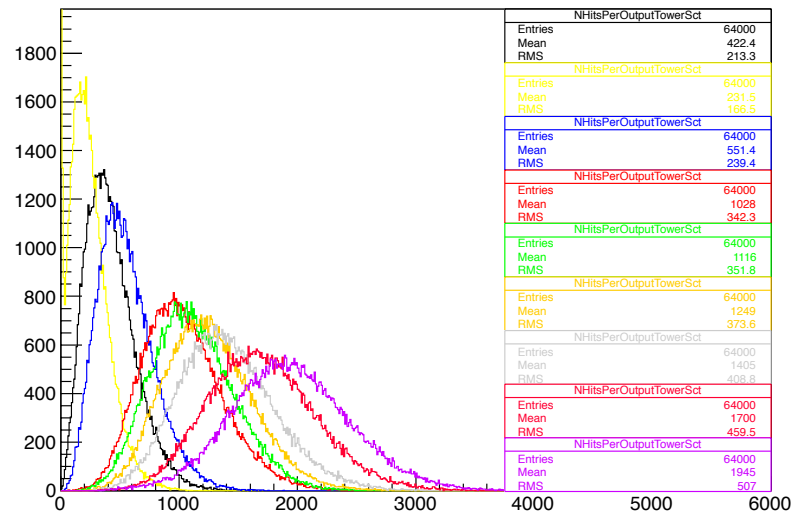
NHitsPerOutputTowerPxl



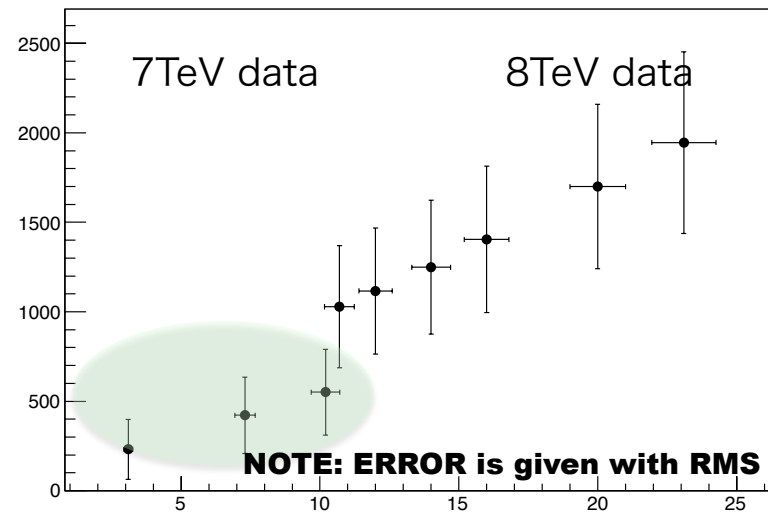
NHitsPerOutputTowerPxl



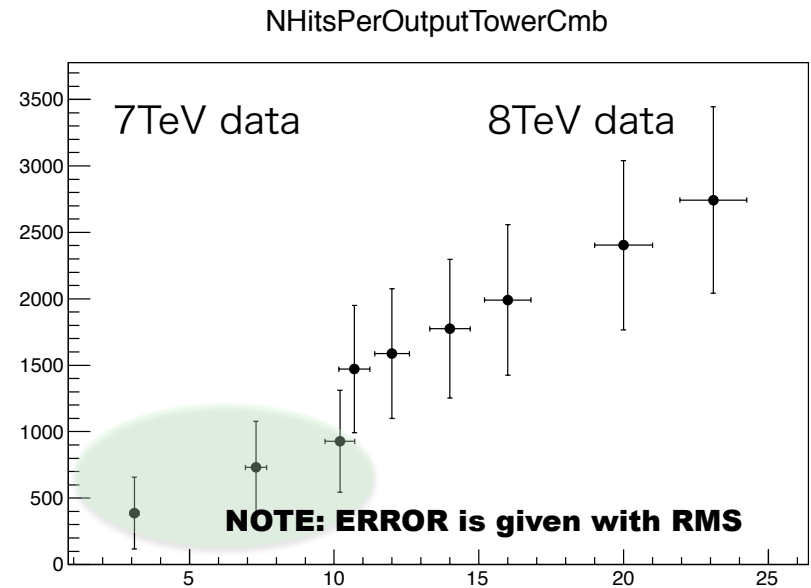
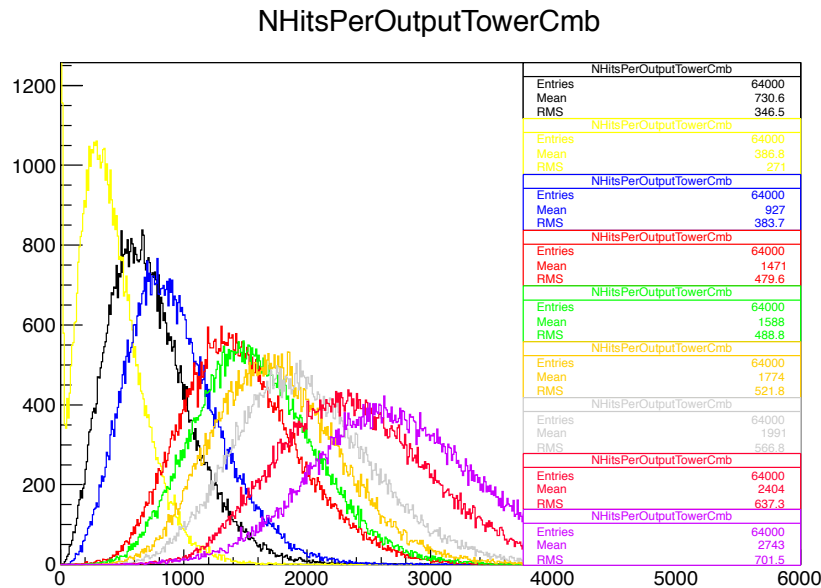
NHitsPerOutputTowerSct



NHitsPerOutputTowerSct



N hits/tower/event (Output)



2,743 hits are input to a FPGA in average with $\langle \mu \rangle = 23$

NOTE :

- A pixel hit is copied & sent to 3.2 towers in average
- A SCT hit is copied & sent to 2.1 towers in average
- 3,000 hits / output line = 10Gbps (still with $\langle \mu \rangle = 23$)
(with assumption of 32bits/hit)